Not Recommended for New Designs
(Suggested Alternate: XRP7714)

XRP7724

Quad Channel Digital PWM/PFM Programmable Power Management System

GENERAL DESCRIPTION

The XRP7724 is a quad channel Digital Pulse Width Modulated (DPWM) Step down (buck) controller. A wide 4.75V to 5.5V and 5.5V to 25V input voltage dual range allows for single supply operation from standard power rails.

With integrated FET gate drivers, two LDOs for standby power and a 105kHz to 1.23MHz independent channel to channel programmable constant operating frequency, the XRP7724 reduces overall component count and solution footprint and optimizes conversion efficiencies. A selectable digital Pulse Frequency Mode (DPFM) capable of better than 80% efficiency at light current load and low operating current allow for portable and Energy Star compliant applications. Each XRP7724 output channel is individually programmable as low as 0.6V with a resolution as fine as 2.5mV, and configurable for precise soft start and soft stop sequencing, including delay and ramp control.

The XRP7724 operations are fully controlled via a SMBus-compliant I^2C interface allowing for advanced local and/or remote reconfiguration, full performance monitoring and reporting as well as fault handling.

Built-in independent output over voltage, over temperature, over-current and under voltage lockout protections insure safe operation under abnormal operating conditions.

The XRP7724 is offered in a RoHS compliant, "green"/halogen free 44-pin TQFN package.

APPLICATIONS

- **Servers**
- **Base Stations**
- **Switches/Routers**
- **Broadcast Equipment**
- **Industrial Control Systems**
- **Automatic Test Equipment**
- **Video Surveillance Systems**

FEATURES

- **Quad Channel Step-down Controller**
  - Digital PWM 105kHz-1.23MHz Operations
  - Individual Channel Frequency Selection
  - Patented digital PFM with Ultrasonic mode
  - Patented Over Sampling Feedback
  - Integrated MOSFET Drivers
  - Programmable 5 coefficient PID control
- **4.75V to 25V Input Voltage**
  - 4.75V-5.5V and 5.5V-25V Input Ranges
  - 0.6V to 5.5V Output voltage
- **SMBus Compliant - I^2C Interface**
  - Full Power Monitoring and Reporting
- **3 x 15V Capable PSIO + 2 x GPIOs**
- **Full Start/Stop Sequencing Support**
- **Built-in Thermal, Over-Current, UVLO and Output Over-Voltage Protections**
- **On Board 5V and 3.3V Standby LDOs**
- **On Board Non-volatile Memory**
- **Supported by PowerArchitect™ Design Tool Version 5 (PA5)**

This Product (or product) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TYPICAL APPLICATION DIAGRAM

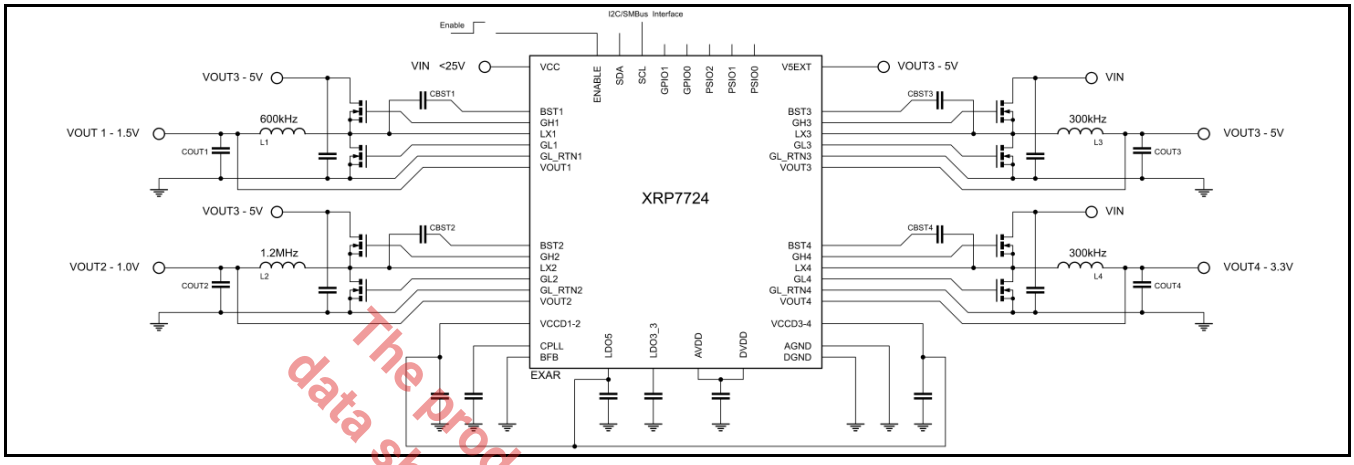

Fig. 1: XRP7724 Application Diagram

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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

VCCD, LDO5, LDO3_3, GLx, VOUTx ..... -0.3V to 7.0V
ENABLE, 5V_EXT ..... -0.3V to 7.0V
GPIO0/1, SCL, SDA 6.0V
PSIOs Inputs, BFB 18V
DVDD, AVDD 2.0V
VCC 28V
LX# ..... -1V to 28V
BSTx, GHx ..... VLXx + 6V
Storage Temperature ..... -65°C to 150°C
Power Dissipation ..... Internally Limited
Lead Temperature (Soldering, 10 sec) ..... 300°C
ESD Rating (HBM - Human Body Model) 2kV

OPERATING RATINGS

Input Voltage Range V_{CC} ..... 5.5V to 25V
Input Voltage Range V_{CC} = LDO5 ..... 4.75V to 5.5V
VOUT1, 2, 3, 4 ..... 5.5V
Junction Temperature Range ..... -40°C to 125°C
JEDEC Thermal Resistance θ_{JA} ..... 30.2°C/W

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ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{CC} = 5.5V to 25V, 5V EXT open. Note that in cases where there is a discrepancy in values shown in this section and other sections of the datasheet, the values in the Electrical Specification section shall be deemed correct and supersede the other values.

QUIESCENT CURRENT

Parameter	Min.	Typ.	Max.	Units		Conditions
VCC Supply Current in SHUTDOWN		10	20	µA		EN = 0V, VCC = 12V
ENABLE Turn On Threshold	0.82		0.95	V		VCC = 12V Enable Rising
ENABLE Pin Leakage Current			10	µA		EN=5V
	-10			µA		EN=0V
VCC Supply Current in STANDBY		440	600	µA		LDO3_3 disabled, all channels disabled GPIOs programmed as inputs VCC=12V,EN = 5V
VCC Supply Current 2ch PFM		3.1		mA		2 channels on set at 5V, VOUT forced to 5.1V, no load, non-switching, Ultra-sonic off, VCC=12 V, No I^2C activity.
VCC Supply Current 4ch PFM		4.0		mA		4 channels on set at 5V, VOUT forced to 5.1V, no load, non-switching, Ultra-sonic off, VCC=12V, No I^2C activity.
VCC Supply Current ON		18		mA		All channels enabled, Fsw=600kHz, gate drivers unloaded, No I^2C activity.

INPUT VOLTAGE RANGE AND UNDERVOLTAGE LOCKOUT

Parameter	Min.	Typ.	Max.	Units		Conditions
VCC Range	5.5		25	V	•	
	4.75		5.5	V	•	With VCC connected to LDO5

VOLTAGE FEEDBACK ACCURACY AND OUTPUT VOLTAGE SET POINT RESOLUTION

Parameter	Min.	Typ.	Max.	Units		Conditions
VOUT Regulation Accuracy Low Output Range 0.6V to 1.6V PWM Operation	-5		5	mV		0.6 ≤ VOUT ≤ 1.6V
	-20		20	mV	•	
	-7.5		7.5	mV		0.6 ≤ VOUT ≤ 1.6V VCC = LDO5
	-22.5		22.5	mV	•	
VOUT Regulation Accuracy Mid Output Range 0.6V to 3.2V PWM Operation	-15		15	mV		0.6 ≤ VOUT ≤ 3.2V
	-45		45	mV	•	
	-20		20	mV		0.6 ≤ VOUT ≤ 3.2V VCC = LDO5
	-50		50	mV	•	
VOUT Regulation Accuracy High Output Range 0.6V to 5.5V PWM Operation	-30		30	mV		0.6 ≤ VOUT ≤ 5.5V
	-90		90	mV	•	
	-40		40	mV		0.6 ≤ VOUT ≤ 4.2V, VIN = 5V VCC = LDO5
	-100		100	mV	•	
VOUT Regulation Range	0.6		5.5	V	•	Without external divider network
VOUT Native Set Point Resolution		12.5 25 50		mV		Low Range Mid Range High Range
VOUT Fine Set Point Resolution[1]		2.5 5 10		mV		Low Range Mid Range High Range
VOUT Input Resistance		120 90 75		kΩ		Low Range Mid Range High Range
VOUT Input Resistance in PFM Operation		10 1 0.67		MΩ		Low Range Mid Range High Range
Power Good and OVP Set Point Range (from set point)	-155 -310 -620		157.5 315 630	mV		Low Range Mid Range High Range
Power Good and OVP Set Point Accuracy	-5 -10 -20		5 10 20	mV		Low Range Mid Range High Range
BFB Set Point Range	9		16	V		
BFB Set Point Resolution		1		V		
BFB Accuracy	-0.5		0.5	V		

Note 1: Fine Set Point Resolution not available in PFM

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CURRENT AND AUX ADC (MONITORING ADCS)

Parameter	Min.	Typ.	Max.	Units		Conditions
Current Sense Accuracy	-3.75	±1.25	3.75	mV		Low Range (≤120mV) Note 2
	-10		10	mV	•	-60mV applied
	-5	±2.5	5	mV		High Range (≤280mV)
	-12.5		+12.5	mV	•	-150mV
Current Sense ADC INL		+/-0.4		LSB		
DNL		0.27				
Current Limit Set Point Resolution and Current Sense ADC Resolution		1.25		mV		Low Range (≤120mV)
		2.5		mV		High Range (≤280mV)
Current Sense ADC Range	-120		20	mV		Low Range (≤120mV)
	-280		40	mV		High Range (≤280mV)
VOUT ADC Resolution		15 30 60		mV		Low Range Mid Range High Range
VOUT ADC Accuracy	-1		1	LSB		
VCC ADC Range	4.6		25	V		Note 3
UVLO WARN SET	4.4		4.72	V		UVLO WARN set point 4.6V, VCC = LDO5
UVLO WARN CLEAR	4.4		4.72	V		UVLO WARN set point 4.6V, VCC = LDO5
UVLO FAULT SET (Note 4)	4.2		4.55	V		UVLO FAULT set point 4.4V, VCC = LDO5
VCC ADC Resolution		200		mV		
VCC ADC Accuracy	-1		1	LSB		Vin <= 20V
Die Temp ADC Resolution		5		°C		
Die Temp ADC Range	-44		156	°C		Output value is in Kelvin

Note 2: Final test limits are ±2.5mV or ±2 LSB
Note 3: Although Range of VCC ADC is technically 0V to 25V, below 4.55 the LDO5 hardware UVLO may have tripped.
Note 4: This test ensures an UVLO FAULT flag will be given before the LDO5 hardware UVLO trips.

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LINEAR REGULATORS

Parameter	Min.	Typ.	Max.	Units		Conditions
LDO5 Output Voltage	4.85	5.0	5.15	V	•	5.5V ≤ VCC ≤ 25V 0mA < $I_{LDO5OUT}$ < 130mA, LDO3_3 Off
LDO5 Current Limit	135	155	180	mA	•	LDO5 Fault Set
LDO5 UVLO	4.74			V	•	VCC Rising
LDO5 PGOOD Hysteresis		375		mV		VCC Falling
LDO5 Bypass Switch Resistance		1.1	1.5	Ω		
Bypass Switch Activation Threshold	2.5		2.5	%	•	V5EXT Rising, % of threshold setting
Bypass Switch Activation Hysteresis		150		mV		V5EXT Falling
LDO3_3 Output Voltage	3.15	3.3	3.45	V	•	4.6V ≤ LDO5 ≤ 5.5V 0mA < I_{LDO3_3OUT} < 50mA
LDO3_3 Current Limit	53		85	mA	•	LDO3_3 Fault Set
Maximum total LDO loading during ENABLE start-up			30	mA		ENABLE transition from logic low to high. Once LDO5 in regulation above limits apply.

PWM Generators and Oscillator

Parameter	Min.	Typ.	Max.	Units		Conditions
Switching Frequency (fsw) Range	105		1230	kHz		Steps defined in table
fsw Accuracy	–5		5	%		
CLOCK IN Synchronization Frequency	20	25.7	31	MHz		When synchronizing to an external clock (Range 1)
CLOCK IN Synchronization Frequency	10	12.8	15.5	MHz		When synchronizing to an external clock (Range 2)

GPIOs[5]

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Pin Low Level			0.8	V		
Input Pin High Level	2.0			V		
Input Pin Leakage Current			1	µA		
Output Pin Low Level			0.4	V		I_{SINK} = 1mA
Output Pin High Level	2.4			V		I_{SOURCE} = 1mA
Output Pin High Level		3.3	3.6	V		I_{SOURCE} = 0mA
Output Pin High-Z leakage Current (GPIO pins only)			10	µA		
Maximum Sink Current			1	mA		Open Drain Mode
I/O Frequency			30	MHz		

Note 5: 3.3V CMOS logic compatible, 5V tolerant.

PSIOs[6]

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Pin Low Level			0.8	V		
Input Pin High Level	2.0			V		
Input Pin Leakage Current			1	µA		
Output Pin Low Level			0.4	V		I_{SINK} = 3mA
Output Pin High Level			15	V		Open Drain. External pull-up resistor to user supply
Output Pin High-Z leakage Current (PSIO pins only)			10	µA		
I/O Frequency			5	MHz		

Note 6: 3.3V/5.0V CMOS logic compatible, maximum rating of 15.0V

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SMBus (I2C) Interface

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Pin Low Level, V_{IL}			0.3 VIO	V		VIO = 3.3 V ±10%
Input Pin High Level, V_{IH}	0.7 VIO			V		VIO = 3.3 V±10%
Hysteresis of Schmitt Trigger inputs, V_{hys}	0.05 VIO			V		VIO = 3.3 V±10%
Output Pin Low Level (open drain or collector), V_{OL}			0.4	V		I_{SINK} = 3mA
Input leakage current	-10		10	µA		Input is between 0.1 VIO and 0.9 VIO
Output fall time from V_{IHmin} to V_{ILmax}	20 + 0.1 Cb		250	ns		With a bus capacitance (Cb)from 10 pF to 400 pF
Internal Pin Capacitance			1	pF		

Gate Drivers

Parameter	Min.	Typ.	Max.	Units		Conditions
GH, GL Rise Time		17		ns		At 10-90% of full scale, 1nF C_{load}
GH, GL Fall Time		11		ns		
GH, GL Pull-Up On-State Output Resistance		4	5	Ω		
GH, GL Pull-Down On-State Output Resistance		2	2.5	Ω		
GH, GL Pull-Down Resistance in Off-Mode		50		kΩ		VCC = VCCD = 0V.
Bootstrap diode forward resistance		9		Ω		@ 10mA
Minimum On Time		50		ns		1nF of gate capacitance.
Minimum Off Time		125		ns		1nF of gate capacitance
Minimum Programmable Dead Time		20		ns		Does not include dead time variation from driver output stage Tsw=switching period
Maximum Programmable Dead Time		Tsw				
Programmable Dead Time Adjustment Step		607		ps		

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BLOCK DIAGRAM

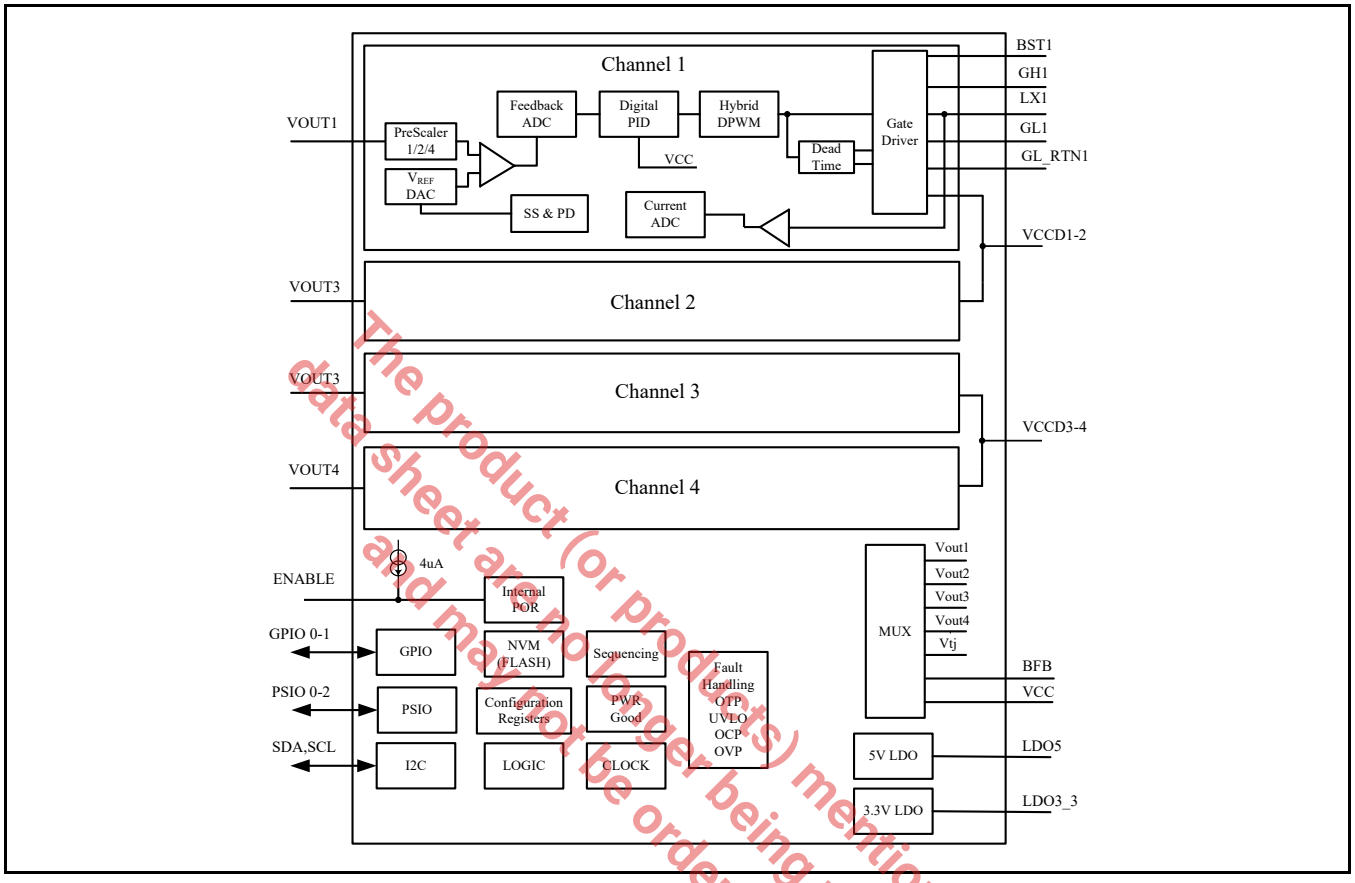

Fig. 2: XRP7724 Block Diagram

LDO BLOCK DIAGRAM

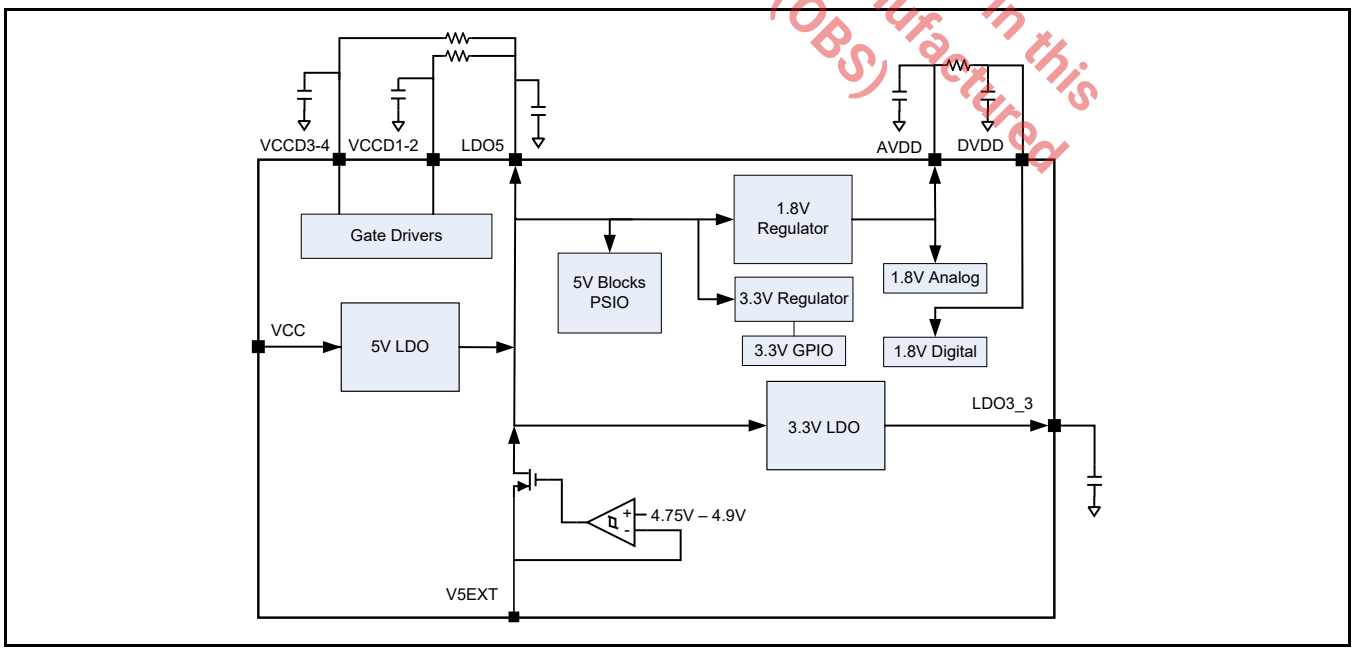

Fig. 3: XRP7724 LDO Block Diagram

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PIN ASSIGNMENT

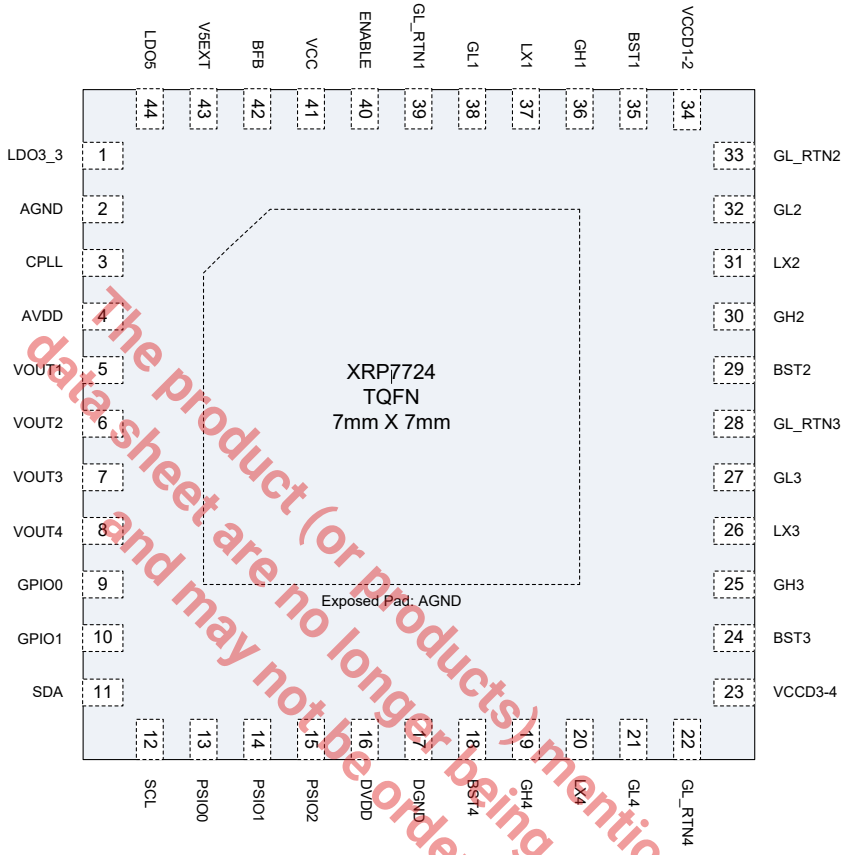

Fig. 4: XRP7724 Pin Assignment

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PIN DESCRIPTION

Name	Pin Number	Description
VCC	41	Input voltage. Place a decoupling capacitor close to the controller IC. This input is used in UVLO fault generation.
DVDD	16	1.8V supply input for digital circuitry. Connect pin to AVDD. Place a decoupling capacitor close to the controller IC.
VCCD1-2 VCCD3-4	23,34	Gate Drive supply. Two independent gate drive supply pins where pin 34 supplies drivers 1 and 2 and pin 23 supplies drivers 3 & 5. One of the two pins must be connected to the LDO5 pin to enable two power rails initially. It is recommended that the other VCCD pin be connected to the output of a 5V switching rail(for improved efficiency or for driving larger external FETs), if available, otherwise this pin may also be connected to the LDO5 pin. A bypass capacitor (>1uF) to PAD is recommended for each VCCD pin with the pin(s) connected to LDO5 with shortest possible length of etch.
AGND	2	Analog ground pin. This is the small signal ground connection.
GL_RTN1- GL_RTN4	39,33, 28,22	Ground connection for the low side gate driver. This should be routed as a signal trace with GL. Connect to the source of the low side MOSFET.
GL1-GL4	38,32, 27,21	Output pin of the low side gate driver. Connect directly to the gate of an external N-channel MOSFET.
GH1-GH4	36,30, 25,19	Output pin of the high side gate driver. Connect directly to the gate of an external N-channel MOSFET.

Name	Pin Number	Description
LX1-LX4	37,31, 26,20	Lower supply rail for the GH high-side gate driver. Connect this pin to the switching node at the junction between the two external power MOSFETs and the inductor. These pins are also used to measure voltage drop across bottom MOSFETs in order to provide output current information to the control engine.
BST1-BST4	35,29, 24,18	High side driver supply pin(s). Connect BST to the external capacitor as shown in the Typical Application Circuit on page 2. The high side driver is connected between the BST pin and LX pin and delivers the BST pin voltage to the high side FET gate each cycle.
GPI0-GPIO1	9,10	These pins can be configured as inputs or outputs to implement custom flags, power good signals, enable/disable controls and synchronization to an external clock.
PSIO0-PSIO2	13,14,15	Open drain, these pins can be used to control external power MOSFETs to switch loads on and off, shedding the load for fine grained power management. They can also be configures as standard logic outputs or inputs just as any of the GPIOs can be configured, but as open drains require an external pull-up when configured as outputs.
SDA, SCL	11,12	SMBus/I^{2}C serial interface communication pins.
VOUT1-VOUT4	5,6,7,8	Connect to the output of the corresponding power stage. The output is sampled at least once every switching cycle
LDO5	44	Output of a 5V LDO. This is a micro power LDO that can remain active while the rest of the IC is in shutdown. This LDO is also used to power the internal Analog Blocks.
LDO3_3	1	Output of the 3.3V standby LDO. This is a micro power LDO that can remain active while the rest of the IC is in shutdown.
ENABLE	40	If ENABLE is pulled high or allowed to float high, the chip is powered up (logic is reset, registers configuration loaded, etc.). The pin must be held low for the XRP7724 to be placed into shutdown.
BFB	42	Input from the 15V output created by the external boost supply. When this pin goes below a pre-defined threshold, a pulse is created on the low side drive to charge this output back to the original level. If not used, this pin should be connected to GND.
DGND	17	Digital ground pin. This is the logic ground connection, and should be connected to the ground plane close to the PAD.
CPLL	3	Connect to a 2.2nF capacitor to GND.
V5EXT	43	External 5V that can be provided. If one of the output channels is configured for 5V, then this voltage can be fed back to this pin for reduced operating current of the chip and improved efficiency.
AVDD	4	Output of the internal 1.8V LDO. A decoupling capacitor should be placed between AVDD and AGND close to the chip.
PAD	45	This is the die attach paddle, which is exposed on the bottom of the part. Connect externally to the ground plane.

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ORDERING INFORMATION[1]

Part Number	Junction Temperature Range	Lead-Free	Package	Packing Method	I^{2}C Default Address
XRP7724ILB-F	-40°C ≤ T_J ≤ +125°C	Yes[2]	44-pin TQFN	Tray	0x28 (7Bit)
XRP7724ILBTR-F				Tape & Reel	
XRP7724EVB-DEMO-2	XRP7724 Evaluation Board				
XR77XXEVB-XCM-V62	Configuration Module				
XRP7724EVB-DEMO-2-KITA	Includes XRP7724EVB-DEMO-2 Evaluation Board, XRP77XXEVB-XCM-V62 Configuration Module and PowerArchitect™ Software				

NOTES:

1. Refer to www.exar.com/XRP7724 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at VCC = 12V, $T_J = T_A$ = 25°C, unless otherwise specified - Schematic and BOM from XRP7724EVB. See XRP7724EVB-DEMO-1 Manual.

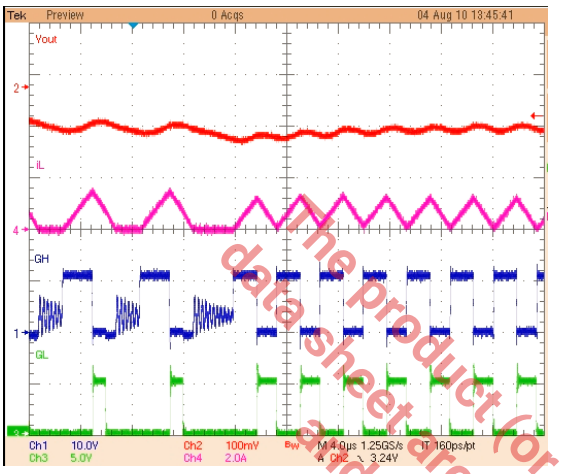

Fig. 5: PFM to PWM Transition

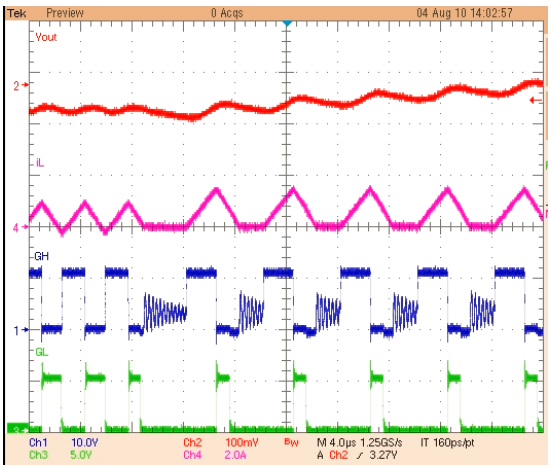

Fig. 6 PWM to PFM Transition

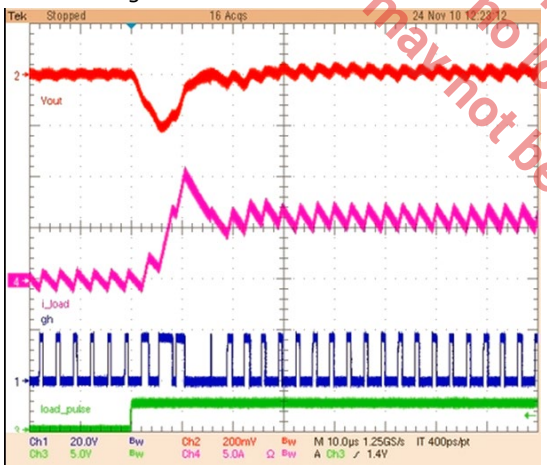

Fig. 7 0-6A Transient 300kHz PWM only

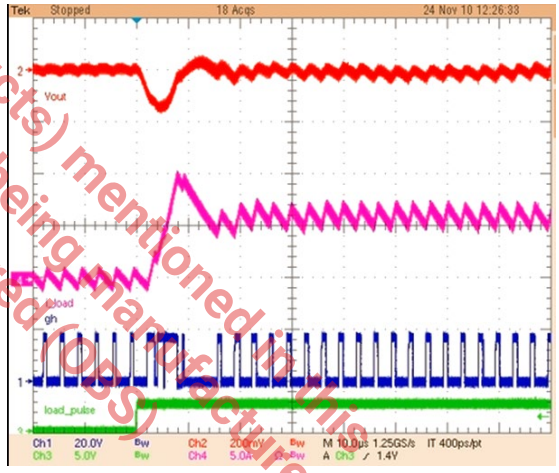

Fig. 8 10-6A Transient 300kHz with OVS ±5.5%

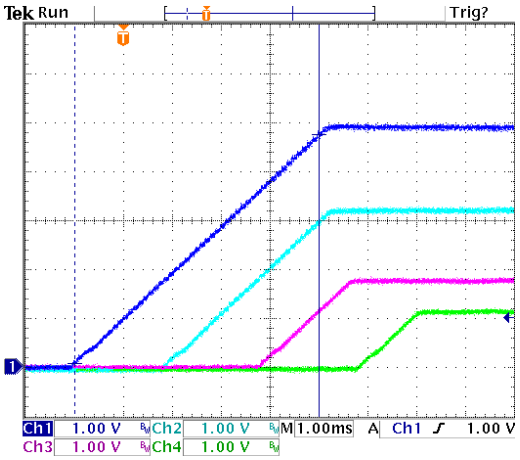

Fig. 9 Sequential Start-up

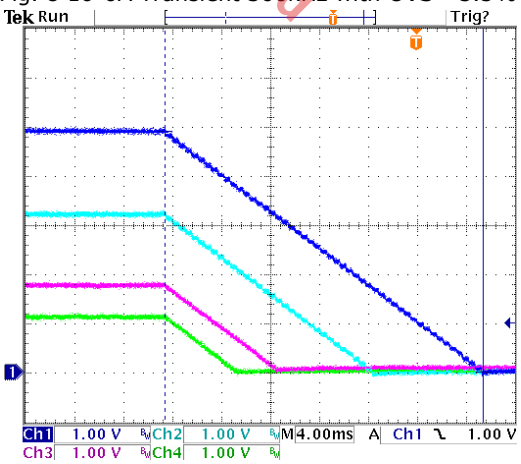

Fig. 10 Sequential Shut Down

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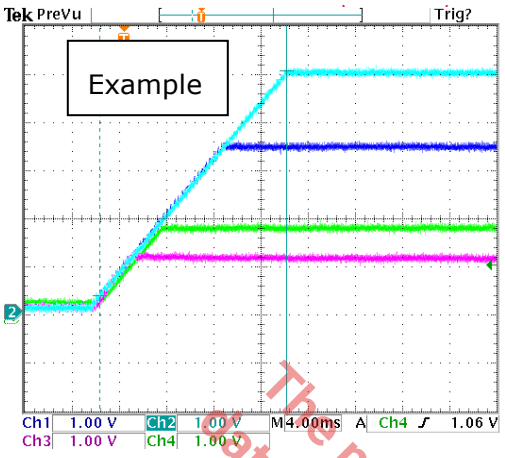

Fig. 11: Simultaneous Start-up

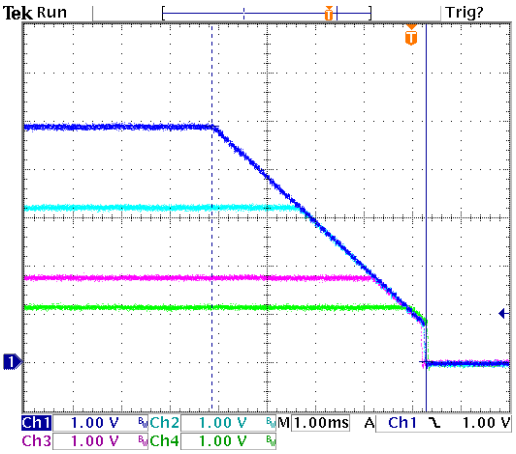

Fig. 12 Simultaneous Shut Down

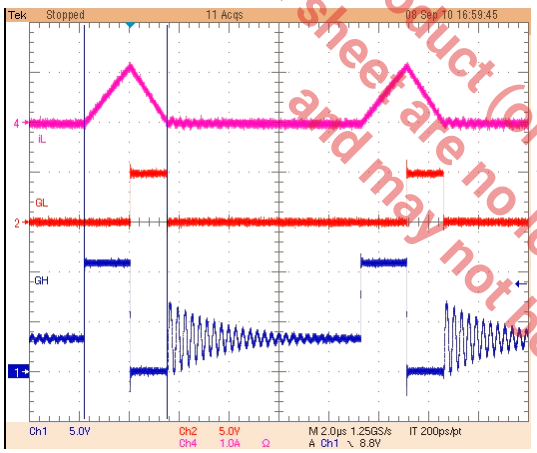

Fig. 13: PFM Zero Current Accuracy

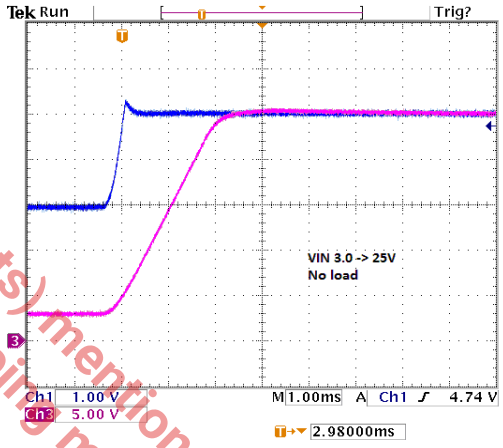

Fig. 14: LDO5 Brown Out Recovery, No Load

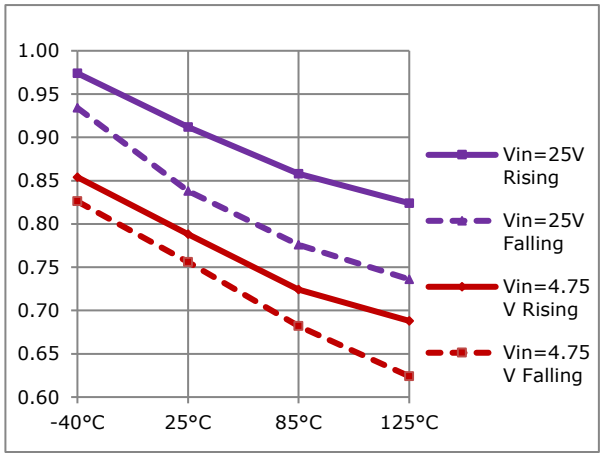

Fig. 15: Enable Threshold Over Temp

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FEATURES AND BENEFITS

Programmable Power Benefits

- **Fully Configurable**
  - Output set point
  - Feedback compensation
  - Frequency set point
  - Under voltage lock out
  - Input voltage measurement
  - Gate drive dead time
- **Reduced Development Time**
  - Configurable and re-configurable for different Vout, Iout, Cout, and Inductor values
  - No need to change external passives for a new output specification.
- **Higher integration and Reliability**
  - Many external circuits used in the past can be eliminated significantly improving reliability.

PowerArchitect™ Design and Configuration Software (PA5)

- Wizard quickly generates a base design
- Calculates all configuration registers
- Projects can be saved and/or recalled
- GPIOs can be configured easily and intuitively
- "Dashboard" Interface can be used for real-time monitoring and debug

System Benefits

- Reliability is enhanced via communication with the system controller which can obtain real time data on an output voltage, input voltage and current.
- System processors can communicate with the XRP7724 directly to obtain data or make adjustments to react to circuit conditions
- A system process or could also be configured to log and analyze operating history, perform diagnostics and if required, take the supply off-line after making other system adjustments.

System Integration Capabilities

- **Single supply operation**
- **I²C interface allows:**
  - Communication with a System Controller or other Power Management devices for optimized system function
  - Access to modify or read internal registers that control or monitor:
    - Output Current
    - Input and Output Voltage
    - Soft-Start/Soft-Stop Time
    - 'Power Good'
    - Part Temperature
    - Enable/Disable Outputs
    - Over Current
    - Over Voltage
    - Temperature Faults
    - Adjusting fault limits and disabling/enabling faults
    - Packet Error Checking (PEC) on I²C communication
- **5 GPIO pins with a wide range of configurability**
  - Fault reporting (including UVLO Warn/Fault, OCP Warn/Fault, OVP, Temperature, Soft-Start in progress, Power Good, System Reset)
  - Allows a Logic Level interface with other non-digital IC's or as logic inputs to other devices
- **Frequency and Synchronization Capability**
  - Selectable switching frequency between 105kHz and 1.2MHz
  - Main oscillator clock and DPWM clock can be synchronized to external sources
  - 'Master', 'Slave' and 'Stand-alone' Configurations are possible
- **Internal MOSFET Drivers**
  - Internal FET drivers (4Ω/2Ω) per channel
  - Built-In Automatic Dead-time adjustment
  - 30ns Rise and Fall times
- **4 Independent SMPS channels and 2 LDOs in a 7x7mm TQFN**

The product (or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OPS).

FUNCTIONAL OVERVIEW

The XRP7724 is a quad-output digital pulse width modulation (DPWM) controller with integrated gate drivers for use with synchronous buck switching regulators. Each output voltage can be programmed from 0.6V to 5.5V without the need of an external voltage divider. The wide range of the programmable DPWM switching frequency (from 105 kHz to 1.2 MHz) enables the user to optimize for efficiency or component sizes. Since the digital regulation loop requires no external passive components, loop performance is not compromised due to external component variation or operating condition.

The XRP7724 provides a number of critical safety features, such as Over-Current Protection (OCP), Over-Voltage Protection (OVP), Over Temperature Protection (OTP) plus input Under Voltage Lockout (UVLO). In addition, a number of key health monitoring features such as warning level flags for the safety functions, Power Goods (PGOOD), etc., plus full monitoring of system voltages and currents. The above are all programmable and/or readable from the SMBus and many are steerable to the GPIOs for hardware monitoring.

For hardware communication, the XRP7724 has two logic level General Purpose Input-Output (GPIO) pins and three, 15V, open drain, Power System Input-Output (PSIO) pins. Two pins are dedicated to the SMBus data (SDA) and clock (SCL). Additional pins include Chip Enable (Enable), Aux Boost Feedback (BFB) and External PLL Capacitor (CPLL).

In addition to providing four switching outputs, the XRP7724 also provides control for an Aux boost supply, and two stand-by linear regulators that produce 5V and 3.3V for a total of 7 customer usable supplies in a single device.

The 5V LDO is used for internal power and is also available for customer use to power external circuitry. The 3.3V LDO is solely for customer use and is not used by the chip. There is also a 1.8V linear which is for internal use only and should not be used externally.

A key feature of the XRP7724 is its powerful power management capabilities. All four outputs are independently programmable and gives the user not only full control of the delay, ramp, and sequence during power up and power down. One can also control of how the outputs interact and power down in the event of a fault. This includes active ramp down of the output voltages to remove an output voltage as quickly as possible. Another nice feature is that the outputs can be defined and controlled as groups.

The XRP7724 has two main types of programmable memory. The first types are runtime registers that contain configuration, control and monitoring information for the chip. The second type is rewritable Non-Volatile Flash Memory (NVFM) that is used for permanent storage of the configuration data along with various chip internal functions. During power up the run time registers are loaded from the NVFM allowing for standalone operation.

The XRP7724 brings an extremely high level of functionality and performance to a programmable power system. Ever decreasing product budgets require the designer to quickly make good cost/performance tradeoffs to be truly successful. By incorporating 4 switching channels, two user LDOs, a charge pump boost controller, along with internal gate drivers, all in a single package, the XRP7724 allows for extremely cost effective power system designs. Another key cost factor to put into the cost tradeoffs, which is often overlooked, is the unanticipated Engineering Change Order (ECO). The programmable versatility of the XRP7724, along with the lack of hard wired, on board configuration components, allows for minor and major changes to be made, in circuit, on the board by simple reprogramming.

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THEORY OF OPERATION

CHIP ARCHITECTURE

REGULATION LOOPS

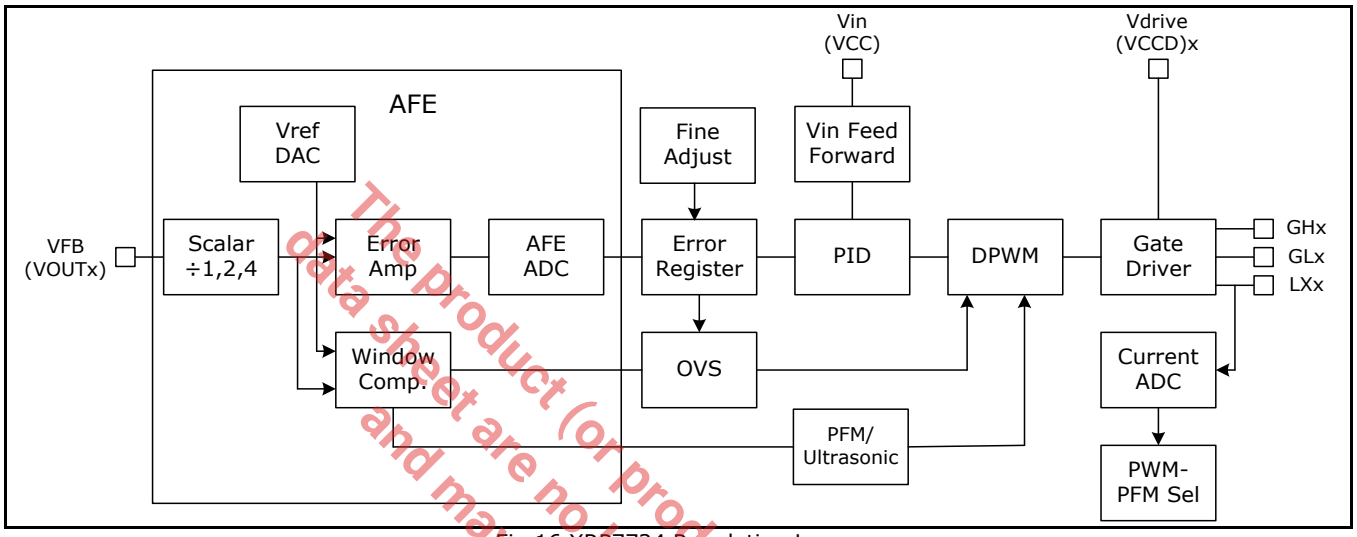

Fig 16 XRP7724 Regulation Loops

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Figure 16 shows a functional block diagram of the regulation loops for an output channel. There are four separate parallel control loops; Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM), Ultrasonic, and Over Sampling (OVS). Each of these loops is fed by the Analog Front End (AFE) as shown at the left of the diagram. The AFE consist of an input voltage scalar, a programmable Voltage Reference (Vref) DAC, Error Amplifier, and a window comparator. (Please note that the block diagram shown is simplified for ease of understanding. Some of the function blocks are common and shared by each channel by means of a multiplexer.)

PWM Loop

The PWM loop operates in Voltage Control Mode (VCM) with optional Vin feed forward based on the voltage at the VCC pin. The reference voltage (Vref) for the error amp is created by a 0.15V to 1.6V DAC that has a 12.5mV resolution. In order to get a full 0.6V to 5.5V output voltage range an input scalar is used to reduce feedback voltages for higher output voltages to bring them within the 0.15V to 1.6V control range. So for output voltages up to 1.6V (low range) the scalar has a gain of 1. For output voltages from 1.6V to 3.2V (mid range) the scalar gain is 1/2 and for voltages greater than 3.2V (high range) the gain is 1/4. This results in the low range having a reference voltage resolution of 12.5mV, mid range of 25mV and the high range having a resolution of 50mV. The error amp has a gain of 4 and compares the output voltage of the scalar to Vref to create an error voltage on its output. This is converted to a digital error term by the AFE ADC which is stored in the error register. The error register has a fine adjust function that can be used to improve the output voltage set point resolution by a factor of 5 resulting in a low range resolution of 2.5mV, mid range resolution of 5mV and a high range resolution of 10mV. The output of the error resister is then used by the Proportional Integral Derivative (PID) controller to manage the loop dynamics.

The XRP7724 PID is a 17-bit five coefficient control engine that calculates the correct duty cycle under the various operating conditions and feeds it to the Digital Pulse Width Modulator (DPWM). Besides the normal coefficients the PID also uses the Vin voltage to provide a feed forward function.

The XRP7724 DPWM includes a special delay timing loop that gives a timing resolution that is 16 times the master oscillator frequency (103MHz) for a timing resolution of 607ps for both the driver pulse width and dead time delays. The DWPM creates and outputs the Gate High (GH) and Gate Low (GL) signals to the driver. The maximum and minimum on times and dead time delays are programmable by configuration resisters.

To provide current information, the output inductor current is measured by a differential amplifier that reads the voltage drop across the RDS of lower FET during its on time. There are two selectable ranges, a low range with a gain of 8 for a +20mV to -120 mV range and a high range with a gain of 4 for +40mV to -280mV range. The optimum range to use will depend on the maximum output current and the RDS of the lower FET. The measured voltage is then converted to a digital value by the current ADC block. The resulting current value is stored in a readable register and also used to determine when PWM to PFM transitions should occur.

PFM mode loop

The XRP7724 has a PFM loop that can be enabled to improve efficiency at light loads. By reducing switching frequency and operating in the discontinuous conduction mode (DCM), both switching and I^2R losses are minimized.

Figure 17 shows a functional diagram of the PFM logic.

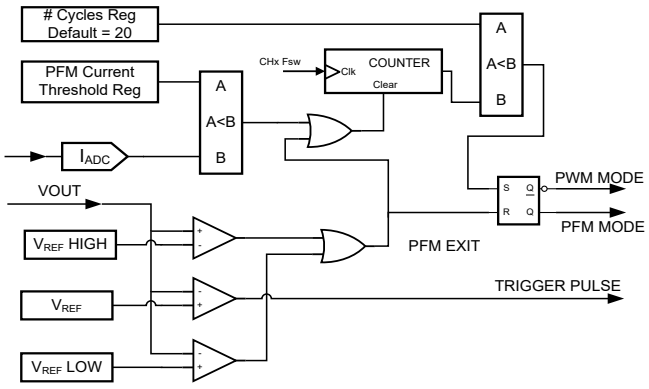

Fig 17: PFM Enter/Exit Functional Diagram

The PFM loop works in conjunction with the PWM loop and is entered when the output current falls below a programmed threshold level for a programmed number of cycles. When PFM mode is entered, the PWM loop is disabled and instead, the scaled output voltage is compared to Vref with a window comparator. The window comparator has three thresholds; normal (Vref), high (Vref + %high) and low (Vref - %low). The %high and %low values are programmable and track Vref.

In PFM mode, the normal comparator is used to regulate the output voltage. If the output voltage falls below the Vref level, the comparator is activated and triggers the DPWM to start a switching cycle. When the high side FET is turned on, the inductor current ramps up which charges up the output capacitors and increasing their voltage. After the completion of the high side and low side on-times, the lower FET is turned off to inhibit any inductor reverse current flow. The load current then discharges the output capacitors until the output voltage falls below Vref and the normal comparator is activated this then triggers the DPWM to start the next switching cycle. The time from the end of the switching cycle to the next trigger is referred to as the dead zone. *This PFM methodology ensures output voltage ripple does not increase from PWM to PFM.*

When PFM mode is initially entered the switching duty cycle is the same that it was in PWM mode. The cause the inductor ripple current to be the same level that it was in PWM mode. During operation the PFM duty cycle is calculated based on the ratio of the output voltage to VCC.

If the output voltage ever goes outside the high/low windows, PFM mode is exited and the PWM loop is reactivated.

Although the PFM mode does a good job in improving efficiency at light load, at very light loads the dead zone time can increase to the point where the switching frequency can enter the audio hearing range. When this happens some components, like the output inductor and ceramic capacitors, can emit audible noise. The amplitude of the noise depends mostly on the board design and on the manufacturer and construction details of the components. Proper selection of components can reduce the sound to very low levels. In general Ultrasonic Mode

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is not used unless required as it reduces light load efficiency.

Ultrasonic Mode

Ultrasonic mode is an extension of PFM to ensure that the switching frequency never enters the audible range. When this mode is entered, the switching frequency is set to 30kHz and the duty cycle of the upper and lower FETs, which are fixed in PFM mode, are decreased as required to keep the output voltage in regulation while maintaining the 30kHz switching frequency.

Under extremely light or zero load currents, the GH on time pulse width can decrease to its minimum width. When this happens, the lower FET on time is increased slightly to allow a small amount of reverse inductor to flow back into Vin to keep the output voltage in regulation while maintaining the switching frequency above the audio range.

Oversampling OVS Mode

Oversampling (OVS) mode is a feature added to the XRP7724 to improve transient responses. This mode can only be enabled when the channel switching frequency is operating in 1x frequency mode. In OVS mode the output voltage is sampled 4 times per switching cycle and is monitored by the AFE window comparator. If the voltage goes outside the set high or low limits, the OVS control electronics can immediately modify the pulse width of the GH or GL drivers to respond accordingly, without having to wait for the next cycle to start. OVS has two types of response depending on whether the high limit is exceeded during an unloading transient (Over Voltage), or the low limit is exceeded during a loading transient (Under Voltage).

Under Voltage OVS: If there is an increasing current load step, the output voltage will drop until the regulator loop adapts to the new conditions to return the voltage to the correct level. Depending on where in the switching cycle the load step happens there can be a delay of up to one switching cycle before the control loop can respond. With OVS enabled if output voltage drops below the lower level, an immediate GH pulse will be generated and sent to the driver to increase the output inductor current toward the new load level without having to wait for the next cycle to begin. If the output voltage is still below the lower limit at the beginning of the next cycle, OVS will work in conjunction with the PID to insert additional GH pulses to quickly return the output voltage back within its regulation band. The result of this system is transient response capabilities on par or exceeding those of a constant on-time control loop.

Over Voltage OVS: When there is a step load current decrease, the output voltage will increase (bump up) as the excess inductor current that is no longer used by the load, flows into the output capacitors causing the output voltage to rise. The voltage will continue to rise until the inductor current decreases to the new load current. With OVS enabled, if the output voltage exceeds the high limit of the window comparator, a blanking pulse is generated to truncate the GH signal. This causes inductor current to immediately begin decreasing to the new load level. The GH will continue to be blanked until the output voltage falls below the high limit. Again, since the output voltage is sampled at four times the switching frequency, over shoot will be decreased and the time required to get back into the regulation band is also decreased.

OVS can be used in conjunction with both the PWM and PFM operating modes. When it is activated it can noticeably decrease output voltage excursions when transitioning between PWM and PFM modes.

INTERNAL DRIVERS

The internal high and low gate drivers use totem pole FETs for high drive capability. They are powered by two external 5V power pins (VCCD1-2) and (VCCD3-4), VCCD1-2 powers the drivers for channels 1 and 2 and VCCD3-4 powers channels 3 and 4. The drivers can be powered by the internal 5V LDO by connecting their power pins to the LDO5 output through an RC filter to avoid conducted noise back into the analog circuitry.

To minimize power dissipation in the 5V LDO it is recommended to power the drivers from an external 5V power source either directly or by

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using the V5EXT input. Good quality 1uF to 4.7uF capacitors should be connected directly between the power pins to ground to optimize driver performance and minimize noise coupling to the 5V LDO supply.

The driver outputs should be connected directly to their corresponding output switching FETs, with the Lx output connected to the drain of the lower FET for the best current monitoring accuracy.

See ANP-32 "Practical Layout Guidelines for Power^{XR} Designs".

LDOs

The XRP7724 has two internal Low Drop Out (LDO) linear regulators that generate 5.0V (LDO5) and 3.3V (LDO3_3) for both internal and external use. Additionally it also has a 1.8V regulator that supplies power for the XRP7724 internal circuits. Figure 3 shows a block diagram of the linear power supplies. LDO5 is the main power input to the device and is supplied by an external 5.5V to 25V.

(VCC) supply. The output of LDO5 should be bypassed by a good quality capacitor connected between the pin and ground close to the device.

The 5V output is used by the XRP7724 as a standby power supply and is also used to power the 3.3V and 1.8V linear regulators inside the chip and can also supply power to the 5V gate drivers. The total output current that the 5V LDO can provide is 130mA. The XRP7724 consumes approximately 20mA and the rest is shared between LDO3_3 and the gate drive currents. *During initial power up, the maximum external load should be limited to 30mA.*

The 3.3V LDO output available on the LDO3_3 pin is solely for customer use and is not used internally. This supply may be turned on or off by the configuration registers. Again a good bypass capacitor should be used.

The AVDD pin is the 1.8V regulator output and needs to be connected externally to the DVDD pin on the device. A good quality capacitor should be connected between this pin and ground close to the package.

For operation with a VCC of 4.75V to 5.5V, the LDO5 output needs to be connected directly to VCC on the board.

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CLOCKS AND TIMING

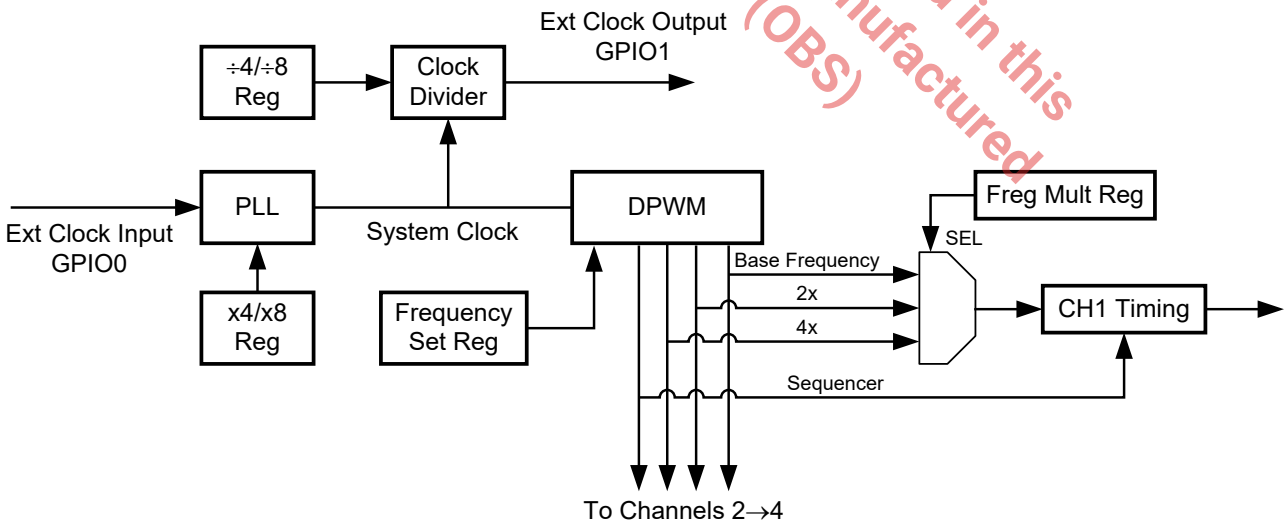

Fig 18 XRP7724 Timing Block Diagram

Figure 18 shows a simplified block diagram of the XRP7724 timings. Again, please note that the function blocks and signal names used are chosen for ease of understanding and do not necessarily reflect the actual design.

The system timings are generated by a 103MHz internal system clock (Sys_Clk). There are two ways that the 103 MHz system clock can be generated. These include an internal oscillator and a Phase Locked Loop (PLL) that is synchronized to an external clock input. The basic timing architecture is to divide the Sys_Clk down to create a fundamental switching frequency (Fsw_Fund) for all the output channels that is settable from 105kHz to 306kHz. The switching frequency for a channel (Fsw_CHx) can then be selected as 1 times, 2 times or 4 times the fundamental switching frequency.

To set the base frequency for the output channels a "Fsw_Set" value representing the base frequency shown in Table 1, is entered into the switching frequency configuration register (Fsw_Set is basically equal to the base frequency times 256). The system timings are then created by dividing down Sys_Clk to produce a base frequency clock, 2X and 4X times the base frequency clocks, and sequencing timing to position the output channels relative to each other. Each output channel then has its own frequency multiplier register that is used to select its final output switching frequency.

Table 1 shows the available channel switching frequencies for the XRP7724 device. In practice the PowerArchitect™ design tool handles all the details and the user only has to enter the fundamental switching frequency and the 1x, 2x, 4x frequency multiplier for each channel.

If an external clock is used, the frequencies in this table will shift accordingly.

Base Frequency kHz	Available 2x Frequencies kHz	Available 4x Frequencies kHz
105.5	211.1	422.1
107.3	214.6	429.2
109.1	218.2	436.4
111.0	222.0	444.0
112.9	225.9	451.8
115.0	229.9	459.8
117.0	234.1	468.2
119.2	238.4	476.9
121.5	242.9	485.8
123.8	247.6	495.2
126.2	252.5	504.9
128.8	257.5	515.0
131.4	262.8	525.5
134.1	268.2	536.5
137.0	273.9	547.9
139.9	279.9	559.8
143.1	286.1	572.2
146.3	292.6	585.2
149.7	299.4	598.8
153.3	306.5	613.1
157.0	314.0	628.0
160.9	321.9	643.8
165.1	330.1	660.3
169.4	338.8	677.6
174.0	348.0	695.9
178.8	357.6	715.3
183.9	367.9	735.7
189.3	378.7	757.4
195.1	390.2	780.3
201.2	402.3	804.7
207.7	415.3	830.6
214.6	429.2	858.3
222.0	444.0	887.9
229.9	459.8	919.6
238.4	476.9	953.7
247.6	495.2	990.4
257.5	515.0	1030.0
268.2	536.5	1072.9
279.9	559.8	1119.6
292.6	585.2	1170.5
306.5	613.1	1226.2

Table 1

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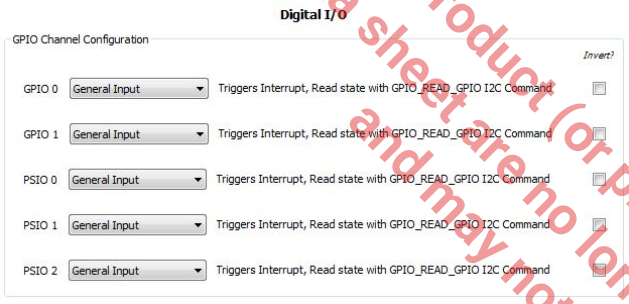
SUPERVISORY AND CONTROL

Power system design with XRP7724 is accomplished using PowerArchitect™ design tool version 5 (PA5). All figures referenced in the following sections are taken from PA5. Furthermore, the following sections reference I²C commands. For more on these commands please refer to ANP-38.

DIGITAL I/O

XRP7724 has two General Purpose Input Output (GPIO) and three Power System Input Output (PSIO) user configurable pins.

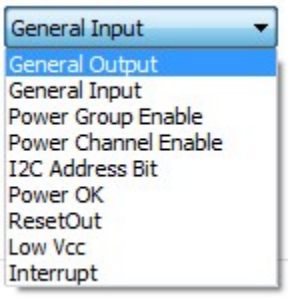


- GPIOs are 3.3V CMOS logic compatible and 5V tolerant.
- PSIO configured as outputs are open drain and require external pull-up resistor. These I/Os are 3.3V and 5V CMOS logic compatible, and up to 15V capable.

The polarity of the GPIO/PSIO pins is set in PA5 or with an I²C command.

Configuring GPIO/PSIOs

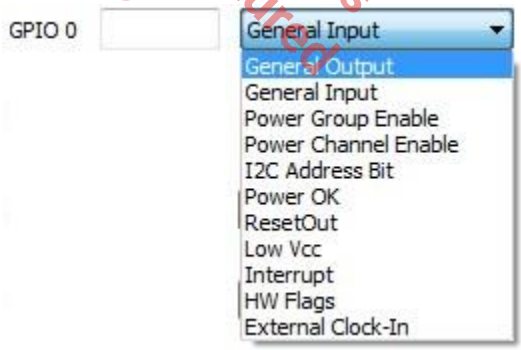
The following functions can be controlled from or forwarded to any GPIO/PSIO:



- **General Output** – set with an I2C command
- **General Input** – triggers an interrupt; state read with an I2C command
- **Power Group Enable** – controls enabling and disabling of Group 1 and Group 2
- **Power Channel Enable** – controls enabling and disabling of a individual channel including LDO3.3
- **I²C Address Bit** – controls an I2C address bit
- **Power OK** – indicates that selected channels have reached their target levels the last time it was powered up. Multiple channel selection is available in which case the resulting signal is the AND logic function of all channels selected
- **ResetOut** – is delayed Power OK. Delay is programmable in 1msec increments with the range of 0 to 255 msecs
- **Low Vcc** – indicates when Vcc has fallen below the UVLO fault threshold and when the UVLO condition clears (Vcc voltage rises above the UVLO warning level)
- **Interrupt** – the controller generated interrupt selection and clearing is done through I²C commands

Interrupt, Low Vcc, Power OK and ResetOut signals can only be forwarded to a single GPIO/PSIO.

In addition, the following are functions that are unique to GPIO0 and GPIO1.



HW Flags – these are hardware monitoring functions forwarded to GPIO0 only. The functions include Under-Voltage Warning, Over- Temperature Warning, Over-Voltage

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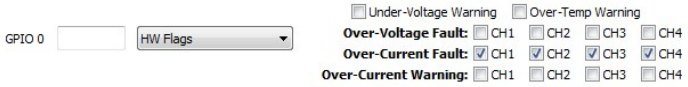
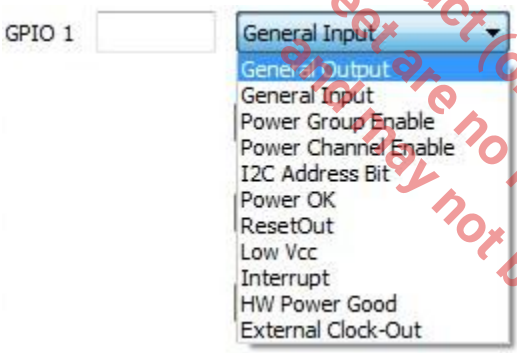
Fault, Over-Current Fault and Over -Current Warning for every channel. Multiple selection is available in which case the resulting signal is the OR logic function

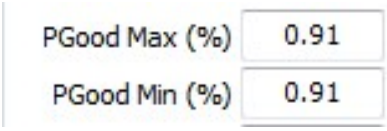


- **External Clock-in** – enables the controller to lock to an external clock including one from another XRP7724 applied to the GPIO0 pin. There are two ranges of clock frequencies the controller accepts, selectable by a user



- **HW Power Good** – the Power Good hardware monitoring function. It can only be forwarded to GPIO1. It is an output voltage monitoring function that is a hardware comparison of channel output voltage against its user defined Power Good threshold limits (Power Good minimum and maximum levels). . It has no hysteresis. Multiple channel selection is available in which case the resulting signal is the AND logic function of all channels selected.

- The Power Good minimum and maximum levels are expressed as percentages of the target voltage.



- "PGood Max" is the upper window and "PGood Min" is the lower window. The minimum and maximum for each of these values can be calculated by the following equation:

$$PGOOD(\%) = \frac{N * LSB(mV)}{Vtarget(V) * 10}$$

- Where N =1 to 63 for the PGOOD Max value and N=1 to 62 for the PGOOD Min value. For example, with the target voltage of 1.5V and set point resolution of 2.5mV (LSB), the Power Good min and max values can range from 0.17% to 10.3% and 0.17% to 10.5% respectively. A user can effectively double the values by changing to the next higher output voltage range setting, but at the expense of reduced set point resolution.
- **External Clock-out** – clock sent out through GPIO1 for synchronizing with another XRP7724 (see the clock out section for more information).

Fault Handling

There are seven different types of fault handling:

- **Under Voltage Lockout (UVLO)** monitors voltage supplied to the Vcc pin and will cause the controller to shutdown all channels if the supply drops to critical levels.
- **Over Temperature Protection (OTP)** monitors temperature of the chip and will cause the controller to shutdown all channels if temperature rises to critical levels.
- **Over Voltage Protection (OVP)** monitors regulated voltage of a channel and will cause the controller to react in a user specified way if the regulated voltage surpasses threshold level.
- **Over Current Protection (OCP)** monitors current of a channel and will cause the controller to react in a user specified way if the current level surpasses threshold level.
- **Start-up Time-out Fault monitors if a channel gets into regulation in a user defined time period**

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- **LDO5 Over Current Protection (LDO5 OCP)** monitor current drawn from the regulator and will cause the controller to be reset if the current exceeds LDO5 limit (155mA typical).
- **LDO3.3 Over Current Protection (LDO3.3 OCP)** monitors current drawn from the regulator and will cause the controller to shut down the regulator if the current exceeds LDO3.3 current limit (65mA typical).

UVLO

Both UVLO warning and fault levels are user programmable and set at 200mV increments in PA5.

When the warning level is reached the controller will generate the UVLO_WARNING_EVENT interrupt. In addition, the host can be informed about the event through HW Flags on GPIO0 (see the Digital I/O section).

When an under voltage fault condition occurs, the XRP7724 outputs are shutdown and the UVLO_FAULT_ACTIVE_EVENT interrupt is generated. In addition, the host can be informed by forwarding the Low Vcc signal to any GPIO/PSIO (see the Digital I/O section). This signal transitions when the UVLO fault occurs. When coming out of the fault, rising Vcc crossing the UVLO fault level will trigger the UVLO_FAULT_INACTIVE_EVENT interrupt.

Once UVLO condition clears (Vcc voltage rises Above or TO the user defined UVLO warning level), the Low Vcc signal will transition and the controller will be reset.

A special attention needs to be paid in the case when Vcc = LDO5 = 4.75V to 5.5V. Since the input voltage ADC resolution is 200mV, the UVLO warning and fault set points are coarse for a 5V input. Therefore, setting the warning level at 4.8V and the fault level at 4.6V may result in the outputs not re-enable until a full 5.0V is reached on Vcc. Setting the warning level to 4.6v and the fault level at 4.4V would likely make UVLO handing as desired, however, below 4.6V the device has a hardware UVLO on LDO5 to ensure proper shutdown of the internal circuitry of the controller. This means the 4.4V UVLO fault level will never occur. A special test has been added to ensure that if UVLO FAULT will

OTP

User defined OTP warning, fault and restart levels are set at 5°C increments in PA5.

When the warning level is reached the controller will generate the TEMP_WARNING_EVENT interrupt. In addition, the host can be informed about the event through HW Flags on GPIO0 (see the Digital I/O section).

When an OTP fault condition occurs, the XRP7724 outputs are shutdown and the TEMP_OVER_EVENT interrupt is generated.

Once temperature reaches a user defined OTP Restart Threshold level, the TEMP_UNDER_EVENT interrupt will be generated and the controller will reset.

OVP

A user defined OVP fault level is set in PA5 and is expressed in percentages of a regulated target voltage.

Resolution is the same as for the target voltage (expressed in percentages). The OVP minimum and maximum values are calculated by the following equation where the range for N is 1 to 63:

$$OVP(\%) = \frac{N * LSB(mV)}{Vtarget(V) * 10}$$

When the OVP level is reached and the fault is generated, the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can use an I2C command to check which channel is at fault.

In addition, OVP fault can be monitored through GPIO0.

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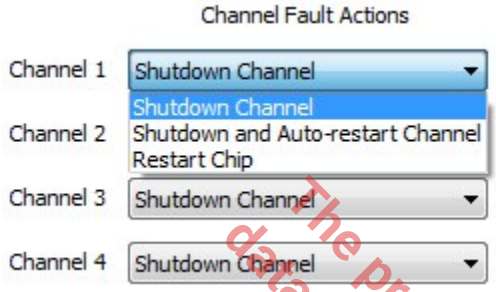
A user can choose one of three options on how to react to an OVP event: to shutdown the faulting channel, to shut down faulting channel and to perform auto-restart of the channel, or to restart the chip.



In the case of shutting down the faulting channel and auto-restarting, the user has an option to specify startup timeout (the time in which the fault is validated) and hiccup timeout (the period after which the controller will try to restart the channel) periods in 1 msec increments with a maximum value of 255 msec.

Startup Timeout (ms)	Hiccup Timeout (ms)
100	100
100	100
100	100
100	100

Note: a channel will share a response to an OVP or OCP event.

OCP

A user defined OCP fault level is set with 1mA increments in PA5. PA5 uses calculations to give the user the approximate DC output current entered in the current limit field. However the actual current limit trip value programmed into the part is limited to 280mV as defined in the electrical characteristics. The maximum value the user can program is limited by Rdson of the synchronous Power FET and current monitoring ADC range. For example, using a synchronous FET with Rdson of 30mΩ, using the wider ADC range, the maximum current limit programmed would be:

$$OCP\ Max(A) = \frac{280mV}{30m\Omega} = 9.33A$$

The current is sampled approximately 30ns before the low side MOSFET turns off, so the actual measured DC output current in this example would be 9.33A plus approximately half the inductor ripple.

An OCP Fault is considered to have occurred only if the fault threshold has been tripped in 4 consecutive switching cycles. When the switching frequency is using the 4x multiplier, the current is sampled only every other cycle. As a result it can take as many as 8 switching cycles for an over current event to be detected. When operating in 4x mode inductors with a soft saturation characteristic are recommended.

When the OCP level is reached and the fault is generated, the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can use an I2C command to check which channel is at fault.

In addition, OCP fault can be monitored through HW Flags on GPIO0. The host can also monitor OCP warning flag through HW Flags on GPIO0. The OCP warning level is calculated by PowerArchitect™ as 85% of the OCP fault level.

A user can choose one of three options on how to react to an OCP event: to shutdown the faulting channel, to shut down faulting channel and to perform auto-restart of the channel, or to restart the chip.

The output current reported by the XRP7724 is processed through a 7 sample median filter in order to reduce noise. The OCP limit is compared against unfiltered ADC output.

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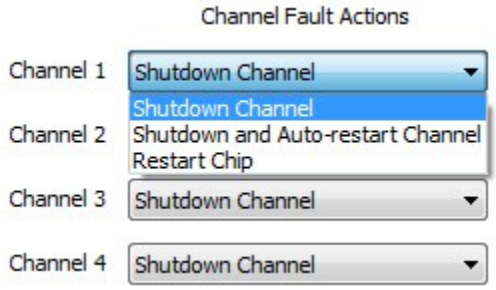


In the case of shutting down the faulting channel and auto-restarting, the user has an option to specify startup timeout (the time in which the fault is validated) and hiccup timeout (the period after which the controller will try to restart the channel) periods in 1 msec increments with a maximum value of 255 msec.

Note: a channel will share a response to an OCP or OVP event.

Start-up Time-out Fault

A channel will be at Start-up Time-out Fault if it does not come-up in a time period specified in the "Startup Timeout" box. In addition, a channel is at Start-up Timeout Fault if in pre-bias configuration voltage is a defined value too close to the target.

When the fault is generated, the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can use an I2C command to check which channel is at fault.

LDO5 OCP

When current is drawn from LDO5 exceeds LDO5 current limit the controller gets reset.

LDO3.3 OCP

When current drawn from LDO3.3 exceeds LDO3.3 current limit the regulator gets shut down, a fault is generated, and the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can through an I2C command check which channel/regulator is at fault. Once the fault condition is removed, the host needs to turn the regulator on again.

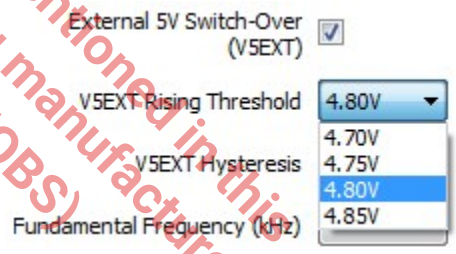
V5EXT SWITCHOVER

The V5EXT gives a user an opportunity to supply an external 5 Volt rail to the controller in order to reduce the controller's power dissipation. The 5 Volt rail can be an independent power rail present in a system or any of 7724 channels regulated to 5 Volts (in the PFM mode in particular) and routed back to the V5EXT pin. It is important to mention that voltage to Vcc must be applied all the time even after the switchover in which case the current drawn from Vcc supply will be minimal.

If the function not used, we recommend the pin to be either grounded or left floating in conjunction with making sure the function gets disabled through register settings.

V5EXT switchover control

The function is enabled in PA5. The switchover thresholds are programmable in 50mV steps with a total range of 200mV. Hysteresis to go in-out is 150mV. LDO5 automatically turns off when the external voltage is switched in and turns on when the external voltage drops below the lower threshold.



When the controller switches over to the V5EXT rail, the V5EXT_RISE interrupt is generated to inform the host. Similarly, when the controller switches out, the V5EXT_FALL interrupt gets generated.

EXTERNAL CLOCK SYNCHRONIZATION

XRP7724 can be run off an external clock available in the system or another XRP7724. The external clock must be in the ranges of 10.9MHz to 14.7MHz or 21.8MHz to 29.6MHz. Locking to the external clock is done through an internal Phase Lock Loop (PLL) which requires an external loop capacitor of 2.2nF to be connected between the CPLL pin and AGND.

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In applications where this functionality is not desired, the CPLL capacitor is not necessary and can be omitted, and the pin shall be left floating. In addition, the user needs to make sure the function gets disabled through register settings.

The external clock must be routed to GPIO0. The GPIO0 setting must reflect the range of the external clock applied to it: Sys_Clock/8 corresponds to the range of 10.9MHz to 14.7MHz while Sys_Clock/4 setting corresponds to the range of 21.8Mhz to 29.6MHz.

The functionality is enabled in PA5 by selecting External Clock-in function under GPIO0.

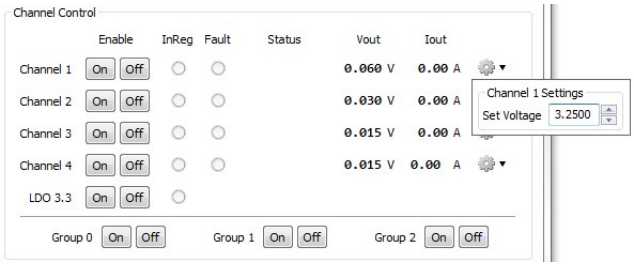
For more on details how to monitor PLL lock in-out, please contact MaxLinear or your local MaxLinear representative.

CLOCK OUT

XRP7724 can supply clock out to be used by another XRP7724 controller. The clock gets routed out through GPIO1 and can be set to system clock divided by 8 (Sys_Clock/8) or system clock divided by 4 (Sys_Clock/4) frequencies.

The functionality is enabled in PA5 by selecting External Clock-Out function under GPIO1.

CHANNEL CONTROL



Channels including LDO3.3 can be controlled independently by any GPIO/PSIO or I2C command. Channels will start-up or shut-down following transitions of signals applied to GPIO/PSIOs set to control the channels. The control can always be overridden with an I2C command.

Regardless whether the channels are controlled independently or are in a group, the ramp rates specified are followed (see the Power Sequencing section).

Regulated voltages and voltage drops across synchronous FET on each switching channel can be read back using x I2C commands y. The regulated voltage read back resolution is 15mV, 30mV and 60mV per LSB depending on the target voltage range. The voltage drop across synchronous FET read back resolution is 1.25mV and 2.5mV per LSB depending on the range.

Through an I2C command the host can check the status of the channels; whether they are in regulation or at fault.

Regulated voltages can be dynamically changed on switching channels using I2C commands with resolution of 2.5mV, 5mV and 10mV depending on the target voltage range (in PWM mode only).

For more information on I2C commands please contact MaxLinear or your local MaxLinear representative.

POWER SEQUENCING

All four channels and LDO3.3 can be grouped together and as such start-up and shut-down in a user defined sequence.

Selecting none means channel(s) will not be assigned to any group and as such will be controlled independently.

Group Selection

There are three groups:

- **Group 0** – is controlled by the chip ENABLE or I2C command. Channels assigned to this group will come up with the ENABLE signal being high, and will go down with the ENABLE signal being low. The control can

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always be overridden with an I2C command.

- Since it is recommended to leave the ENABLE pin floating in the applications when Vcc = LDO5 = 4.75V to 5.5V, please contact MaxLinear for how to configure the channels to come up at the power up in this scenario.
- **Group 1** – can be controlled by any GPIO/PSIO or I2C command. Channels assigned to this group will start-up or shut-down following transitions of a signal applied to the GPIO/PSIO set to control the group. The control can always be overridden with an I2C command.
- **Group 2** – can be controlled by any GPIO/PSIO or I2C command. Channels assigned to this group will start-up or shut-down following transitions of a signal applied to the GPIO/PSIO set to control the group. The control can always be overridden with an I2C command.

Start-up

For each channel within a group a user can specify the following start-up characteristics:

- **Ramp Rate** – expressed in milliseconds per Volt. It does not apply to LDO3.3.
- **Order** – order position of a channel to come-up within the group
- **Wait PGOOD?** – selecting this option for a channel means the next channel in the order cannot start ramping-up until this channel reaches the target level and its Power Good flag gets asserted.
- **Delay** – an additional time delay a user can specify to postpone a channel start-up with respect to the previous channel in the order. The delay is expressed in milliseconds with a range of 0msec to 255msec.

Shut-down

For each channel within a group a user can specify the following shut-down characteristics:

- **Ramp Rate** – expressed in milliseconds per Volt. It does not apply to LDO3.3.
- **Order** – order position of a channel to come-down within the group
- **Wait Stop Thresh?** – selecting this option for a channel means the next channel in the order cannot start ramping-down until this channel reaches the Stop Threshold level. The stop threshold level is fixed at 600mV.
- **Delay** – additional time delay a user can specify to postpone a channel shut-down with respect to the previous channel in the order. The delay is expressed in milliseconds with a range of 0msec to 255msec.

Monitoring Vcc and Temperature

Through I2C commands, the host can read back voltage applied to the Vcc pin and the die temperature respectively. The Vcc read back resolution is 200mV per LSB; the die temperature read back resolution is 5°C per LSB. For more on I2C commands please refer to ANP-38 "XRP7724 Command Set and Programming Guide".

Programming XRP7724

XRP7724 is a FLASH based device which means its configuration can be programmed into FLASH NVM and re-programmed a number of times.

Programming of FLASH NVM is done through PA5.

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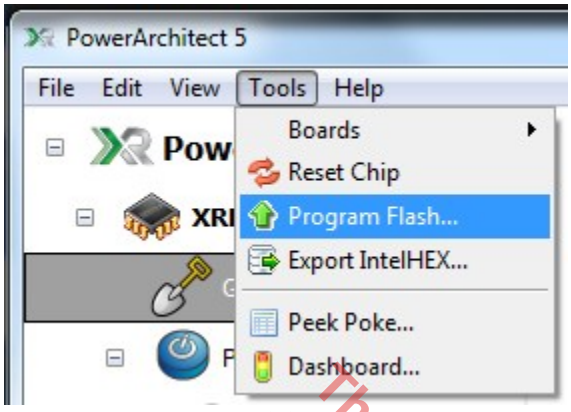
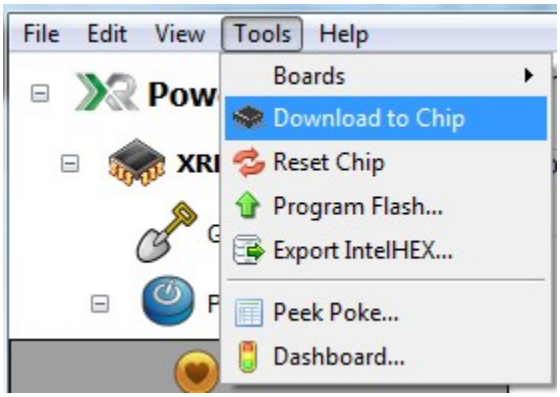
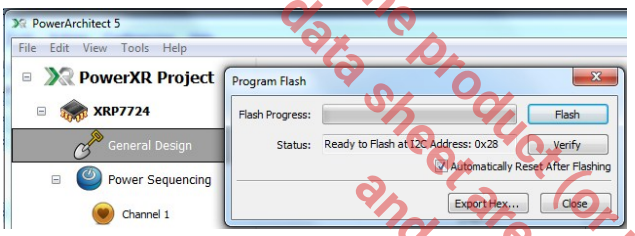
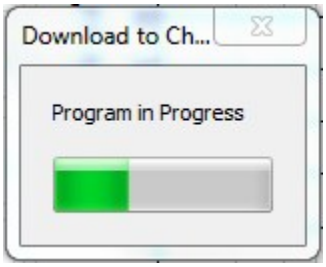
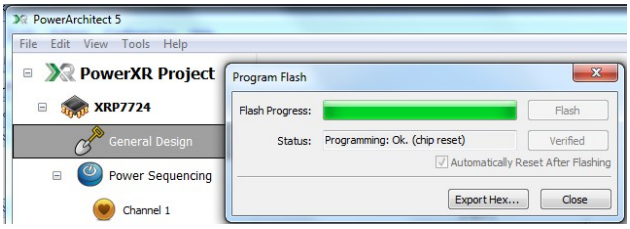








By clicking on the Flash button, user will start programming sequence of the design configuration into the Flash NVM. After the programming sequence completes, the chip will reset (if automatically reset After Flashing box is checked), and boot the design configuration from the Flash.



For users that wish to create their own programming procedure so they can re-program Flash in-circuit using their system software, please contact MaxLinear for a list of I2C Flash Commands needed.

During a design process a user might want to repeatedly download a design configuration onto run time registers without saving it in Flash. This is done through PA5 as well.

ENABLING XRP7724

XRP7724 has a weak internal pull-up ensuring it gets enabled as soon as internal voltage supplies have ramped up and are in regulation.

Driving the Enable pin low externally will keep the controller in the shut-down mode. A simple open drain pull down is the recommended way to shut XRP7724 down.

If the Enable pin is driven high externally to control XRP7724 coming out of the shut-down mode, care must be taken in such a scenario to ensure the Enable pin is driven high after Vcc gets supplied to the controller.

In the configuration when Vcc = LDO5 = 4.75V to 5.5V, disabling the device by grounding the Enable pin is not recommended. At this time we recommend leaving the Enable pin floating and placing the controller in the "Standby Mode" instead in this scenario. The standby mode is defined as the state when all switching channels and LDO3.3 are disabled, all GPIO/PSIOs are programmed as inputs, and system clock is disabled. In this state chip consumes 440uA typical.

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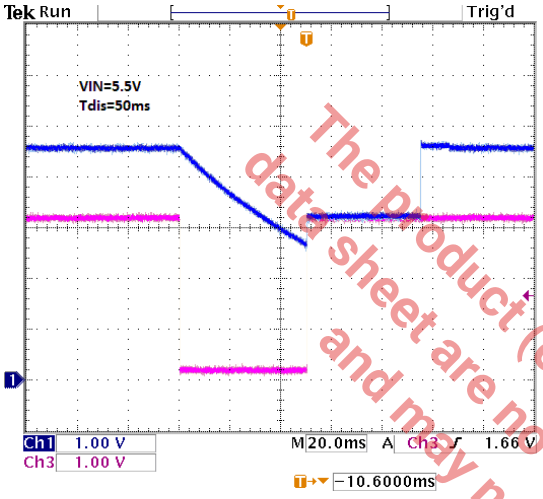
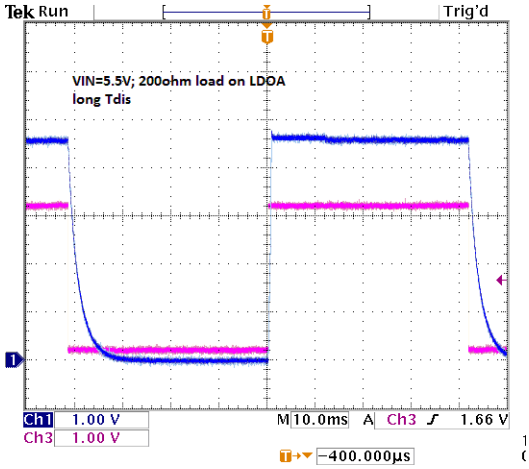
Short duration Enable pin toggled low

Short duration shutdown pulses to the ENABLE pin of the XRP7724 which does not provide sufficient time for the LDO5 voltage to fall below 3.5V can result in significant delay in re-enabling of the device. Some examples below show LDO5 and ENABLE pins:



No load on LDO5, blue trace. Recovery time after ENABLE logic high is approximately 40ms.



Adding a 200 ohm load on LDO5 pulls voltage below 3.5V and restart is short.

Note that as V_{CC} increases, the restart time falls as well. 5.5V input is shown as the worst case.

Since the ENABLE pin has an internal current source, a simple open drain pull down is the recommended way to shut down the XRP7724. A diode in series with a resistor between the LDO5 and ENABLE pins may offer a way to more quickly pull down the LDO5 output when the ENABLE pin is pulled low.

APPLICATION INFORMATION

THERMAL DESIGN

As a 4 channel controller with internal MOSFET drivers and 5V gate drive supply all in one 7x7mm 44pin TQFN package, there is the potential for the power dissipation to exceed the package thermal limitations. The XRP7724 has an internal LDO which supplies 5V to the internal circuitry and MOSFET drivers during startup. It is generally expected that either one of the switching regulator outputs is 5V or another 5V rail is available in the system and connected to the 5V EXT pin. If there is no 5V available in the system, then the power loss will increase significantly and proper thermal design becomes critical. For lower power levels using properly sized MOSFETs, the use of the internal 5V regulator as a gate drive supply is considered appropriate.

LAYOUT GUIDELINES

Refer to application note ANP-32 "Practical Layout Guidelines for Power^{XR} Designs".

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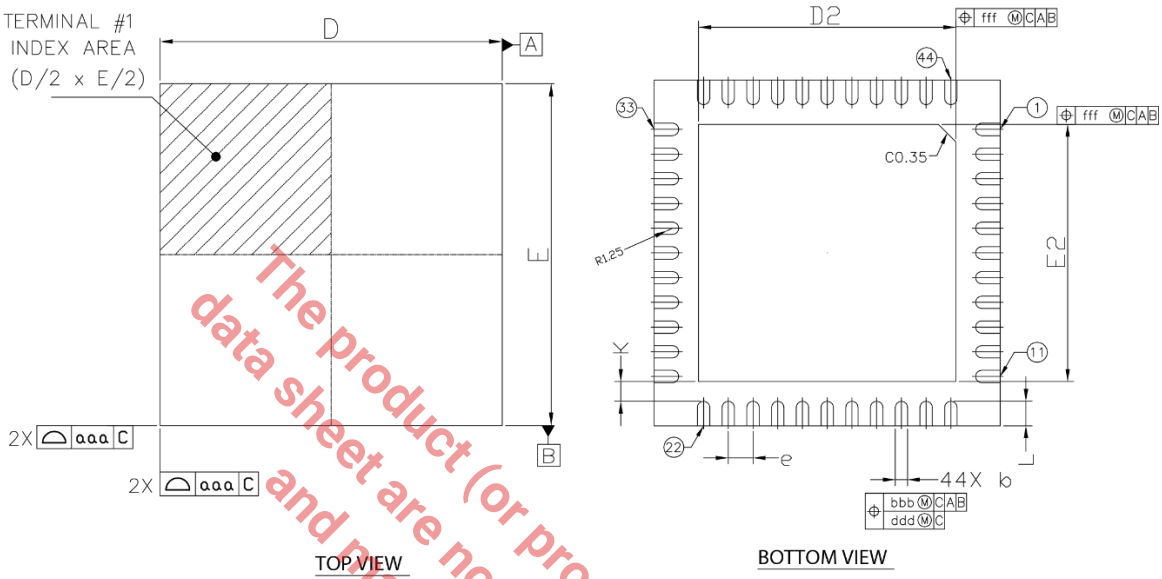
MECHANICAL DIMENSIONS

44-PIN 7X7MM TQFN



DIM / SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20Ref	
b	0.18	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
D2	5.00	5.15	5.30
E2	5.00	5.15	5.30
L	0.40	0.50	0.60
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		44	

TERMINAL DETAILS

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

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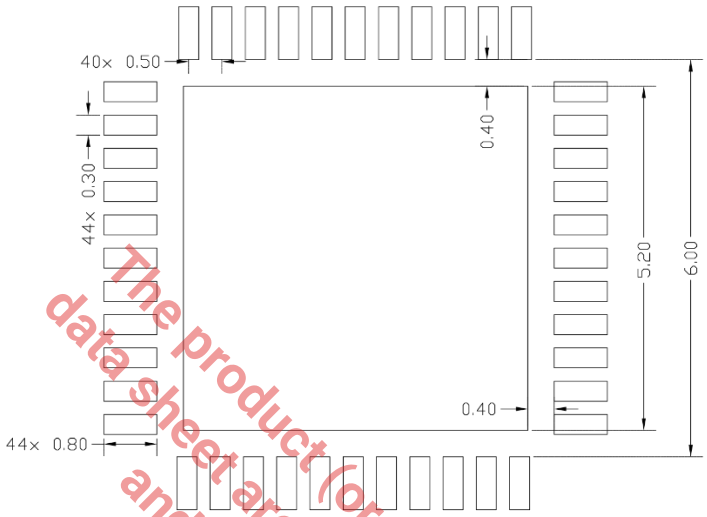
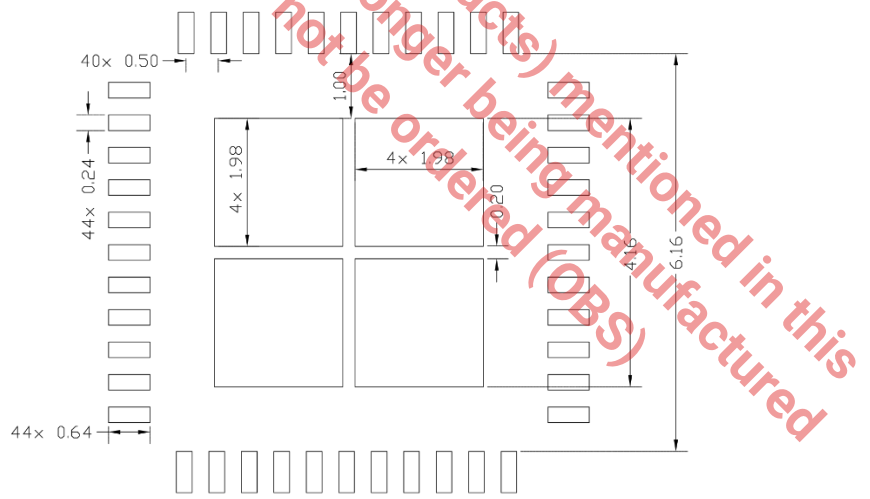
RECOMMENDED LAND PATTERN AND STENCIL

44-PIN 7X7MM TQFN



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000049

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REVISION HISTORY

Revision	Date	Description
1.0.0	10/04/2012	Initial Release of Data Sheet
1.0.1	10/04/2012	Eliminated "Native GH, GL Rise and Fall Time" typical specification.
1.0.2	02/06/19	Updated to Maxlinear logo. Updated format and Ordering Information. Clarified VOUT Regulation Accuracy High Output Range conditions. Added missing units for ENABLE pin Leakage Current and Current Sense ADC Range. Corrected 607ns timing resolution in PWM Loop section to 607ps. Corrected pin names in LDOs section. Updated Power OK description in Configuring GPIO / PSIOs section. Updated PGOOD and OVP equation format. Added "PA5" naming to PowerArchitect™ 5.0.

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