EXAR

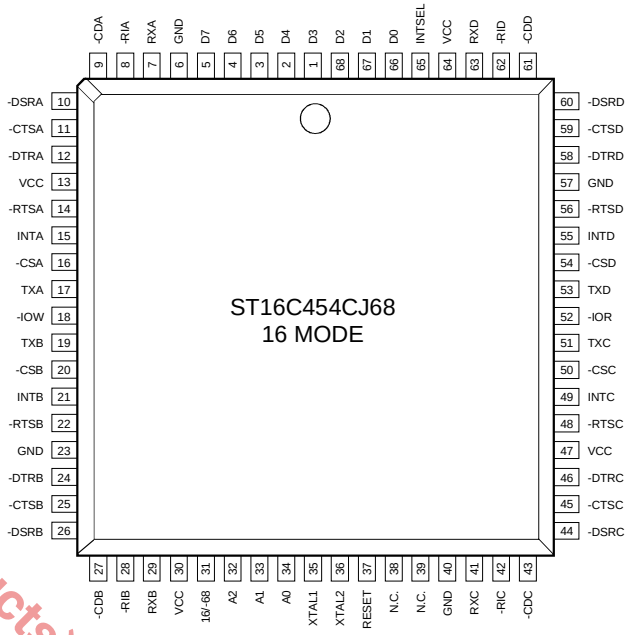
QUAD UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

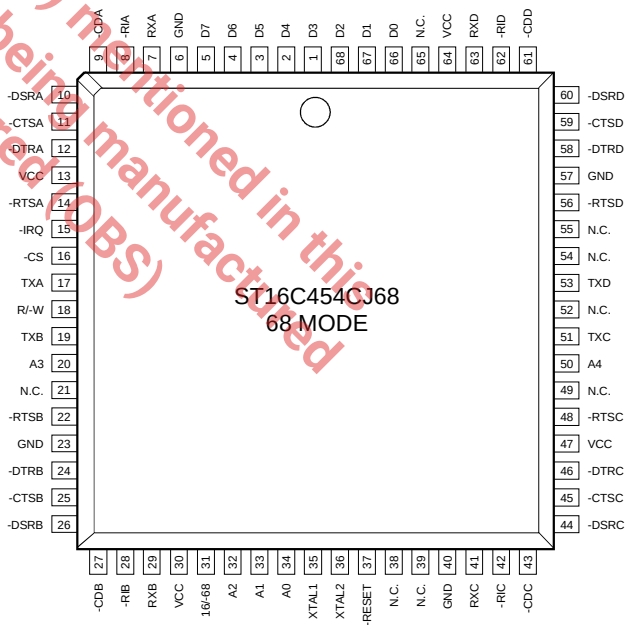
DESCRIPTION

The ST16C454 is a universal asynchronous receiver and transmitter (UART) with a dual foot print interface. The 454 is an enhanced UART with data rates up to 1.5Mbps and software compatible to ST16C450. Onboard status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. The ST16C454 offer an additional 68 mode which allows easy integration with Motorola, and other popular microprocessors. The 454 combines the package interface modes of the ST16C454 on a single integrated chip with a selection pin.

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PLCC Package





FEATURES

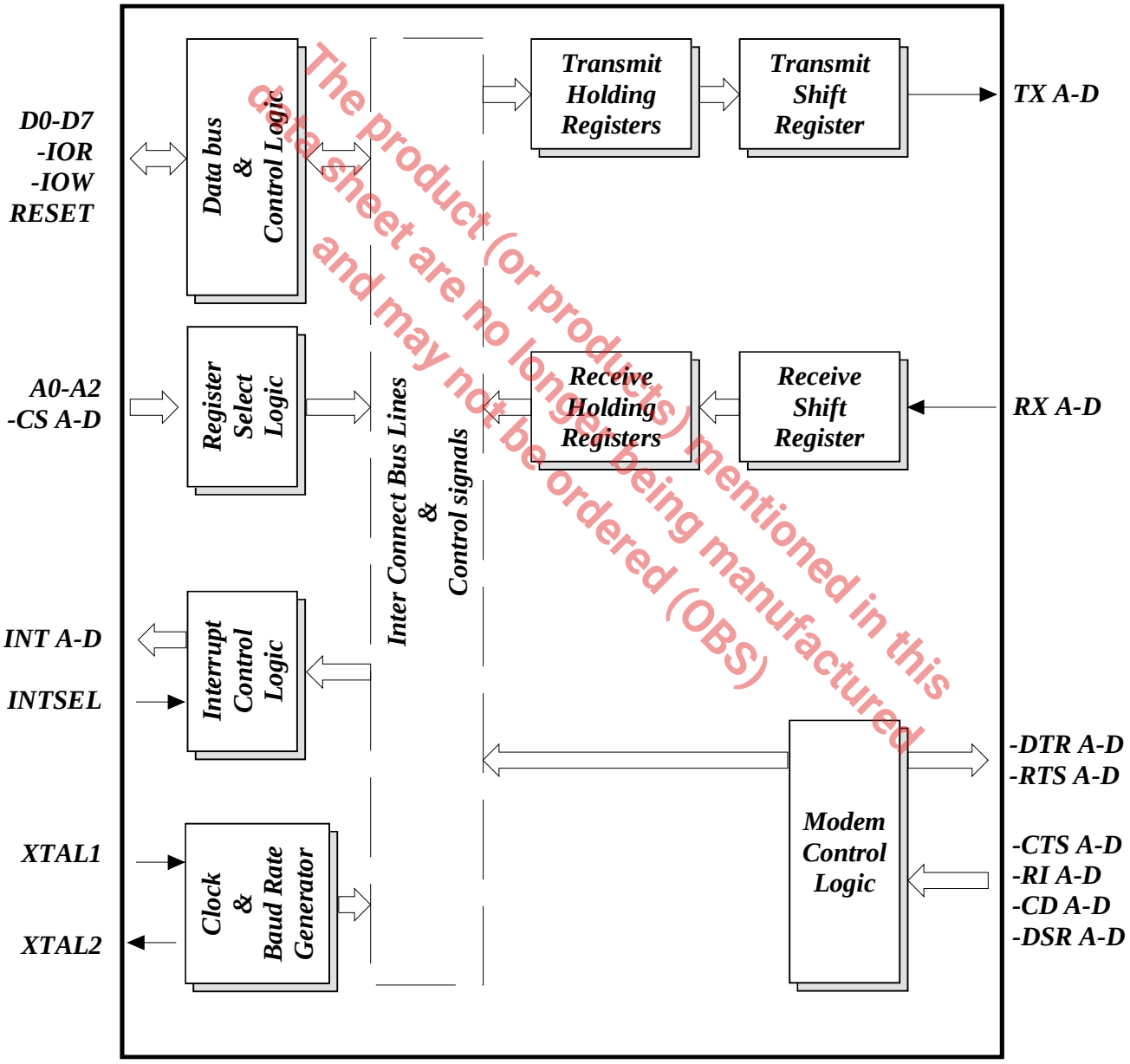
- Software compatibility with the Industry Standard 16C450
- 2.97 to 5.5 volt operation
- Intel or Motorola data bus interface select
- 1.5 Mbps transmit/receive operation (24MHz)
- Independent transmit and receive control
- Software selectable Baud Rate Generator
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Internal loop-back diagnostics
- TTL compatible inputs, outputs
- Low power

ORDERING INFORMATION

Part number	Package	Operating temperature	Device Status
ST16C454CJ68	68-Lead PLCC	0° C to + 70° C	Active
ST16C454IJ68	68-Lead PLCC	-40° C to + 85° C	Active

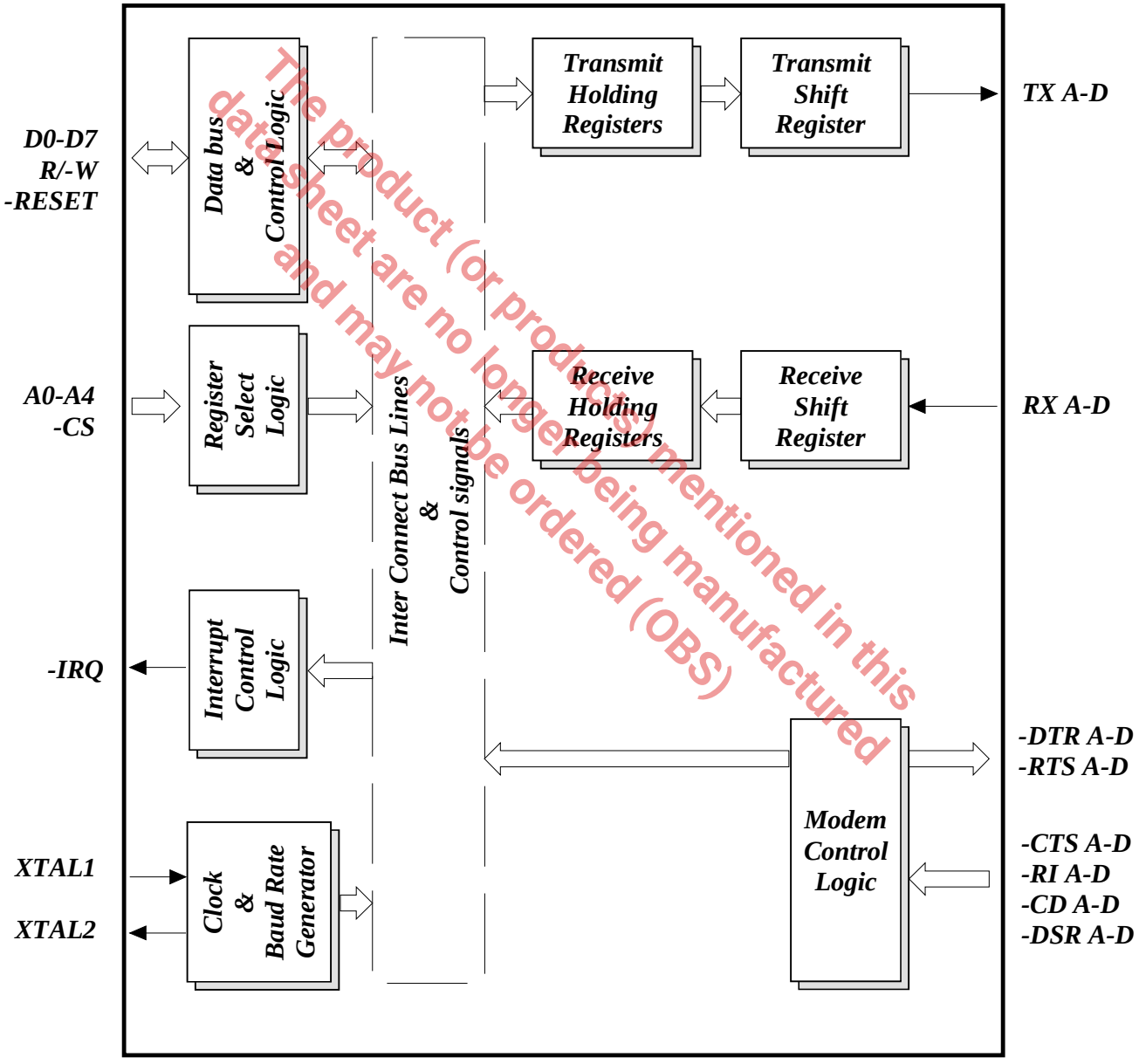
EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 • (510) 668-7000 • FAX (510) 668-7017

Figure 2, Block Diagram in 16 Mode



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Figure 3, Block Diagram in 68 Mode



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin Description
16/-68	31	I	16/68 Interface Type Select (input with internal pull-up). - This input provides the 16 (Intel) or 68 (Motorola) bus interface type select. The functions of -IOR, -IOW, INT A-D, and -CS A-D are re-assigned with the logical state of this pin. When this pin is a logic 1, the 16 mode interface ST16C454 is selected. When this pin is a logic 0, the 68 mode interface (ST68C454) is selected. When this pin is a logic 0, -IOW is re-assigned to R/-W, RESET is re-assigned to -RESET, -IOR is not used, and INT A-D(s) are connected in a WIRE-OR" configuration. The WIRE-OR outputs are connected internally to the open source IRQ signal output.
A0	34	I	Address-0 Select Bit. Internal registers address selection in 16 and 68 modes.
A1	33	I	Address-1 Select Bit. Internal registers address selection in 16 and 68 modes.
A2	32	I	Address-2 Select Bit. - Internal registers address selection in 16 and 68 modes.
A3-A4	20,50	I	Address 3-4 Select Bits. - When the 68 mode is selected, these pins are used to address or select individual UART's (providing -CS is a logic 0). In the 16 mode, these pins are reassigned as chip selects, see -CSB and -CSC.
-CS	16	I	Chip Select. (active low) - In the 68 mode, this pin functions as a multiple channel chip enable. In this case, all four UART's (A-D) are enabled when the -CS pin is a logic 0. An individual UART channel is selected by the data contents of address bits A3-A4. When the 16 mode is selected, this pin functions as -CSA, see definition under -CS A-B.
-CS A-B -CS C-D	16,20 50,54	I	Chip Select A, B, C, D (active low) - This function is associated with the 16 mode only, and for individual channels, "A" through "D." When in 16 Mode, these pins enable data transfers between the user CPU and the ST16C454 for the channel(s) addressed. Individual UART sections (A, B, C, D) are addressed by providing a logic 0 on the respective -CS A-D pin. When the 68 mode is selected, the functions of these pins are reassigned. 68 mode functions are described under the their respective name/pin headings.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin Description
D0-D2 D3-D7	66-68 1-5	I/O	Data Bus (Bi-directional) - These pins are the eight bit, three state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
GND GND	6,23 40,57	Pwr	Signal and power ground.
INT A-B INT C-D	15,21 49,55	O	Interrupt A, B, C, D (active high) - This function is associated with the 16 mode only. These pins provide individual channel interrupts, INT A-D. INT A-D are enabled when MCR bit-3 is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected. When the 68 mode is selected, the functions of these pins are reassigned. 68 mode functions are described under the their respective name/pin headings.
INTSEL	65	I	Interrupt Select. (active high, with internal pull-down) - This function is associated with the 16 mode only. When the 16 mode is selected, this pin can be used in conjunction with MCR bit-3 to enable or disable the three state interrupts, INT A-D or override MCR bit-3 and force continuous interrupts. Interrupt outputs are enabled continuously by making this pin a logic 1. Making this pin a logic 0 allows MCR bit-3 to control the three state interrupt output. In this mode, MCR bit-3 is set to a logic “1” to enable the three state outputs. This pin is disabled in the 68 mode.
-IOR	52	I	Read strobe. (active low Strobe) - This function is associated with the 16 mode only. A logic 0 transition on this pin will load the contents of an Internal register defined by address bits A0-A2 onto the ST16C454 data bus (D0-D7) for access by an external CPU. This pin is disabled in the 68 mode.
-IOW	18	I	Write strobe. (active low strobe) - This function is associated with the 16 mode only. A logic 0 transition on this pin will transfer the contents of the data bus (D0-D7) from the external CPU to an internal register that is defined by address bits A0-A2. When the 16 mode is selected, this pin functions as R/-W, see definition under

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SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin Description
			R/-W.
-IRQ	15	O	Interrupt Request or Interrupt "A" - This function is associated with the 68 mode only. In the 68 mode, interrupts from UART channels A-D are WIRE-OR'ed" internally to function as a single IRQ interrupt. This pin transitions to a logic 0 (if enabled by the interrupt enable register) whenever a UART channel(s) requires service. Individual channel interrupt status can be determined by addressing each channel through its associated internal register, using -CS and A3-A4. In the 68 mode an external pull-up resistor must be connected between this pin and VCC. The function of this pin changes to INTA when operating in the 16 mode, see definition under INTA.
-RESET RESET	37	I	Reset. - In the 16 mode a logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See ST16C454 External Reset Conditions for initialization details.) When 16/-68 is a logic 0 (68 mode), this pin functions similarly but, as an inverted reset interface signal, -RESET.
R/-W	18	I	Read/Write Strobe (active low) - This function is associated with the 68 mode only. This pin provides the combined functions for Read or Write strobes. A logic 1 to 0 transition transfers the contents of the CPU data bus (D0-D7) to the register selected by -CS and A0-A4. Similarly a logic 0 to 1 transition places the contents of a 454 register selected by -CS and A0-A4 on the data bus, D0-D7, for transfer to an external CPU.
VCC VCC	13 47,64	I	Power supply inputs.
XTAL1	35	I	Crystal or External Clock Input - Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit (see figure 8). Alternatively, an external clock can be connected to this pin to provide custom data rates (see Baud Rate Generator Programming).
XTAL2	36	O	Output of the Crystal Oscillator or Buffered Clock - (See also XTAL1). Crystal oscillator output or buffered clock output.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin Description
-CD A-B -CD C-D	9,27 43,61	I	Carrier Detect (active low) - These inputs are associated with individual UART channels A through D. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
-CTS A-B -CTS C-D	11,25 45,59	I	Clear to Send (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on the -CTS pin indicates the modem or data set is ready to accept transmit data from the 454. Status can be tested by reading MSR bit-4.
-DSR A-B -DSR C-D	10,26 44,60	I	Data Set Ready (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation. This pin has no effect on the UART's transmit or receive operation.
-DTR A-B -DTR C-D	12,24 46,58	O	Data Terminal Ready (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates that the 454 is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR bit-0 will set the -DTR output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR bit-0. This pin has no effect on the UART's transmit or receive operation.
-RI A-B -RI C-D	8,28 42,62	I	Ring Indicator (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
-RTS A-B -RTS C-D	14,22 48,56	O	Request to Send (active low) - These outputs are associated with individual UART channels, A through D. A logic 0 on the -RTS pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register (MCR bit-1) will set this pin to a logic 0 indicating data is available. After a reset this pin will be set to a logic 1. This pin has no effect on the UART's transmit

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SYMBOL DESCRIPTION

Symbol	Pin	Signal type	Pin Description
			or receive operation.
RX A-B RX C-D	7,29 41,63	I	Receive Data Input RX A-D. - These inputs are associated with individual serial channel data to the ST16C454. The RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the RX input pin is disabled and TX data is internally connected to the UART RX Input, internally.
TX A-B TX C-D	17,19 51,53	O	Transmit Data - These outputs are associated with individual serial transmit channel data from the 454. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the TX input pin is disabled and TX data is internally connected to the UART RX Input.

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GENERAL DESCRIPTION

The 454 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The ST16C454 represents such an integration with greatly enhanced features. The 454 is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The 454 combines the package interface modes of the ST16C454 and ST68C454 series on a single integrated chip. The 16 mode interface is designed to operate with the Intel type of microprocessor bus while the 68 mode is intended to operate with Motorola, and other popular microprocessors.

The 454 is capable of operation to 1.5Mbps with a 24 MHz crystal or external clock input. With a crystal of 14.7464 MHz, the user can select data rates up to 921.6Kbps.

The rich feature set of the 454 is available through internal registers. Selectable TX and RX baud rates, modem interface controls. In the 16 mode INTSEL and MCR bit-3 can be configured to provide a software controlled or continuous interrupt capability.

FUNCTIONAL DESCRIPTIONS

Interface Options

Two user interface modes are selectable for the 454 package. These interface modes are designated as the “16 mode” and the “68 mode.” This nomenclature corresponds to the early ST16C454 and ST68C454 package interfaces respectively.

The 16 Mode Interface

The 16 mode configures the package interface pins for connection as a standard 16 series (Intel) device and operates similar to the standard CPU interface available on the ST16C454. In the 16 mode (pin 16/-68 logic 1) each UART is selected with individual chip select (-CSx) pins as shown in Table 2 below.

Table 2, SERIAL PORT CHANNEL SELECTION GUIDE, 16 MODE INTERFACE

-CSA	-CSB	-CSC	-CSD	UART CHANNEL
1	1	1	1	None
0	1	1	1	A
1	0	1	1	B
1	1	0	1	C
1	1	1	0	D

The 68 Mode Interface

The 68 mode configures the package interface pins for connection with Motorola, and other popular microprocessor bus types. The interface operates similar to the ST68C454. In this mode the 454 decodes two additional addresses, A3-A4 to select one of the four UART ports. The A3-A4 address decode function is used only when in the 68 mode (16/-68 logic 0), and is shown in Table 3 below.

Table 3, SERIAL PORT CHANNEL SELECTION GUIDE, 68 MODE INTERFACE

-CS	A4	A3	UART CHANNEL
1	N/A	N/A	None
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D

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Internal Registers

The 454 provides 12 internal registers for monitoring and control. These resisters are shown in Table 4 below. These registers are similar to those already available in the standard 16C450. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user assessable scratchpad register (SPR). Register functions are more fully described in the following paragraphs.

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Table 4, INTERNAL REGISTER DECODE

A2	A1	A0	READ MODE	WRITE MODE
General Register Set (THR/RHR, IER/ISR, MCR/MSR, LCR/LSR, SPR):				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
Baud Rate Register Set (DLL/DLM): Note *2				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch

Note *2: These registers are accessible only when LCR bit-7 is set to a logic 1.

Programmable Baud Rate Generator

The 454 supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example a 33.6Kbps modem that employs data compression may require a 115.2Kbps input data rate. A 128.0Kbps ISDN modem that supports data compression may need an input data rate of 460.8Kbps. The 454 can support a standard data rate of 921.6Kbps.

Single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 24 MHz, as required for supporting a 1.5Mbps data rate. The 454 can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/ 22-33 pF load) is connected externally between the XTAL1 and XTAL2 pins (see figure 8). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. (see Baud Rate Generator Programming).

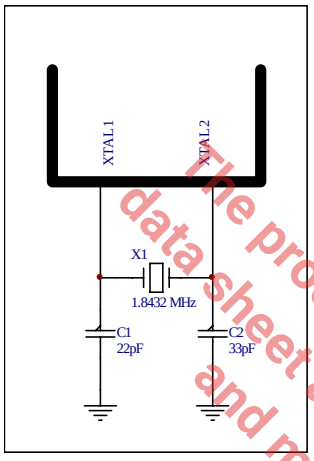
The generator divides the input 16X clock by any divisor from 1 to 2^{16}-1. The 454 divides the basic crystal or external clock by 16. Further division of this 16X clock provides two table rates to support low and high data rate applications using the same system design. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 below, shows the two selectable baud rate tables available when using a 1.8432MHz or 7.3728 MHz crystal.

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Output Baud Rate (1.8432 MHz Clock)	Output Baud Rate (7.3728 MHz Clock)	User 16 x Clock Divisor (Decimal)	User 16 x Clock Divisor (HEX)	DLM Program Value (HEX)	DLL Program Value (HEX)
50	200	2304	900	09	00
300	1200	384	180	01	80
600	2400	192	C0	00	C0
1200	4800	96	60	00	60
2400	9600	48	30	00	30
4800	19.2K	24	18	00	18
9600	38.4k	12	0C	00	0C
19.2k	76.8k	6	06	00	06
38.4k	153.6k	3	03	00	03
57.6k	230.4k	2	02	00	02
115.2k	460.8k	1	01	00	01

Figure 8, Crystal oscillator connection



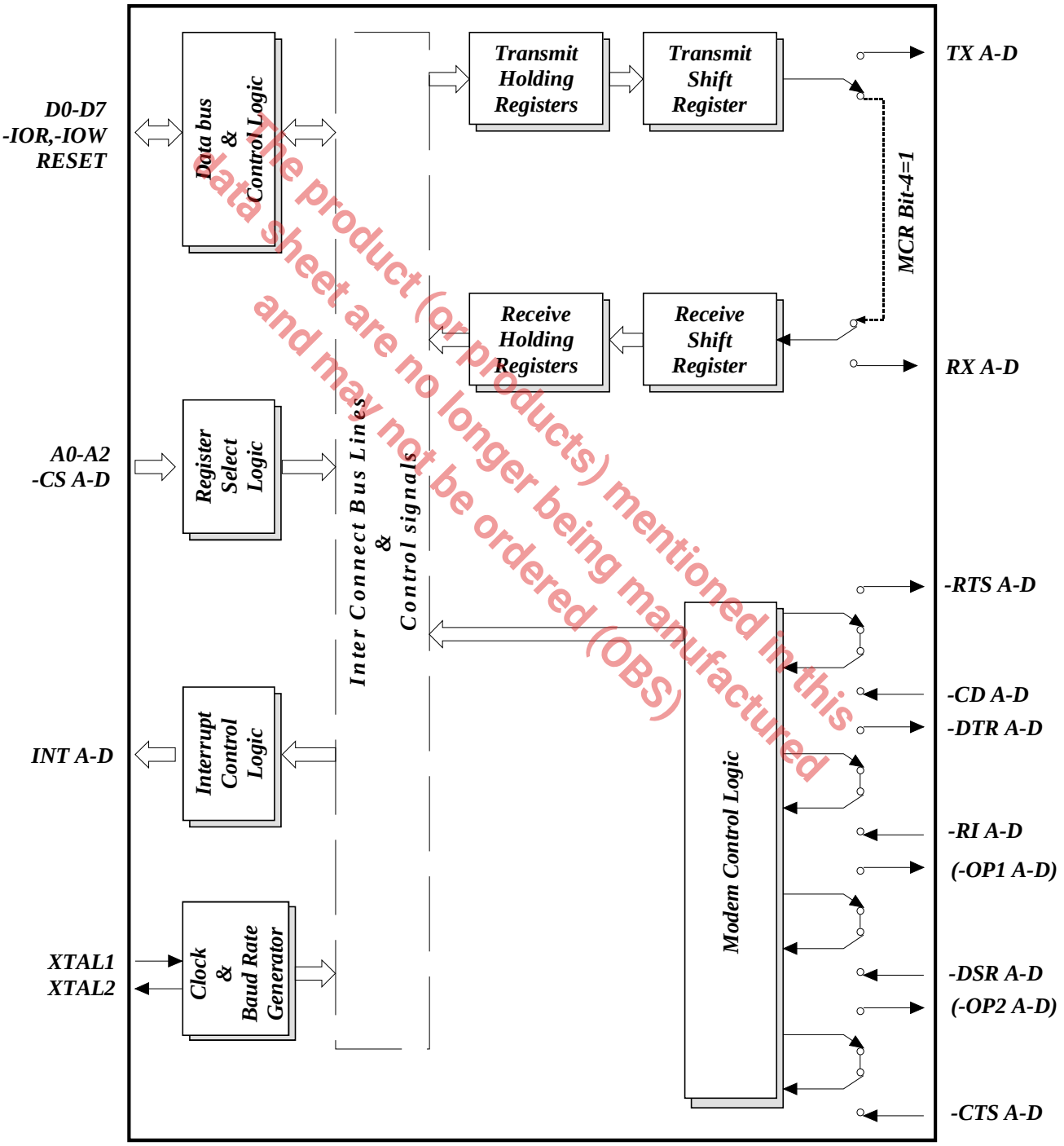
Loop-back Mode

The internal loop-back capability allows onboard diagnostics. In the loop-back mode the normal modem interface pins are disconnected and reconfigured for loop-back internally. MCR register bits 0-3 are used for controlling loop-back diagnostic testing. In the loop-back mode OP1 and OP2 in the MCR register (bits 3/2) control the modem -RI and -CD inputs respectively. MCR signals -DTR and -RTS (bits 0-1) are used to control the modem -CTS and -DSR inputs respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (See Figure 12). The -CTS, -DSR, -CD, and -RI are disconnected from their normal modem control inputs pins, and instead are connected internally to -DTR, -RTS, -OP1 and -OP2. Loop-back test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface, D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Control Register (MCR bits 0-3) instead of the four Modem Status Register bits 4-7. The interrupts are still controlled by the IER.

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Figure 12, INTERNAL LOOP-BACK MODE DIAGRAM



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REGISTER FUNCTIONAL DESCRIPTIONS

The following table delineates the assigned bit functions for the fifteen 454 internal registers. The assigned bit functions are more fully defined in the following paragraphs.

Table 6, ST16C454 INTERNAL REGISTERS

A2 A1 A0	Register [Default] Note *5	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
General Register Set									
0 0 0	RHR[XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR[XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER[00]	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR[01]	0	0	0	0	INT priority bit-2	INT priority bit-1	INT priority bit-0	INT status
0 1 1	LCR[00]	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR[00]	0	0	0	loop back	-OP2/ INTx enable	-OP1	-RTS	-DTR
1 0 1	LSR[60]	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR[X0]	CD	RI	DSR	CTS	delta -CD	delta -RI	delta -DSR	delta -CTS
1 1 1	SPR[FF]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Special Register set: Note *2									
0 0 0	DLL[XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM[XX]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

Note *2: The Special register set is accessible only when LCR bit-7 is set to “1”.

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Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the transmit holding register empty flag is set.

The serial receive section also contains an 8-bit Receive Holding Register, RHR. Receive data is removed from the 454 by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at 16x clock rate. After 7 1/2 clocks the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT A-D output pins in the 16 mode, or on WIRE-OR IRQ output pin, in the 68 mode.

IER BIT-0:
This interrupt will be issued when the RHR is full, cleared when the RHR is empty.
Logic 0 = Disable the receiver ready interrupt. (normal default condition)
Logic 1 = Enable the receiver ready interrupt.

IER BIT-1:
This interrupt will be issued whenever the THR is empty and is associated with bit-1 in the LSR register.
Logic 0 = Disable the transmitter empty interrupt. (normal default condition)
Logic 1 = Enable the transmitter empty interrupt.

IER BIT-2:
This interrupt will be issued whenever a fully assembled receive character is transferred from the RSR to the RHR, data ready, LSR bit-0.
Logic 0 = Disable the receiver line status interrupt. (normal default condition)
Logic 1 = Enable the receiver line status interrupt.

IER BIT-3:
Logic 0 = Disable the modem status register interrupt. (normal default condition)
Logic 1 = Enable the modem status register interrupt.

IER BIT 4-7:
Not used - Initialized to a logic 0.

Interrupt Status Register (ISR)

The 454 provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after rereading the interrupt status bits. The Interrupt Source Table 7 (below) shows the data values (bit 0-5) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels:

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Table 7, INTERRUPT SOURCE TABLE

Priority Level	[ISR BITS] Bit-3	Bit-2	Bit-1	Bit-0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
Logic 1 = No interrupt pending. (normal default condition)

ISR BIT 1-3: (logic 0 or cleared is the default condition)
These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (See Interrupt Source Table).

ISR BIT 4-7:
Not used - Initialized to a logic 0.

Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR BIT 0-1: (logic 0 or cleared is the default condition)
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2: (logic 0 or cleared is the default condition)
The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	Word length	Stop bit length (Bit time(s))
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
Logic 0 = No parity. (normal default condition)
Logic 1 = A parity bit is generated during the transmission, receiver checks the data and parity for transmission errors.

LCR BIT-4:
If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.
Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted data. The receiver must be programmed to check the same format. (normal default condition)
Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted. The receiver must be programmed to check the same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

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LCR BIT-5 = logic 0, parity is not forced. (normal default condition)
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

LCR Bit-5	LCR Bit-4	LCR Bit-3	Parity selection
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity "1"
1	1	1	Forced parity "0"

LCR BIT-6:
When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR bit-6 to a logic 0.
Logic 0 = No TX break condition. (normal default condition)
Logic 1 = Forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition.

LCR BIT-7:
Not used - Initialized to a logic 0.

Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

MCR BIT-0:
Logic 0 = Force -DTR output to a logic 1. (normal default condition)
Logic 1 = Force -DTR output to a logic 0.

MCR BIT-1:
Logic 0 = Force -RTS output to a logic 1. (normal default condition)
Logic 1 = Force -RTS output to a logic 0.

MCR BIT-2:
This bit is used in the Loop-back mode only. In the loop-back mode this bit is use to write the state of the modem -RI interface signal via -OP1.

*MCR BIT-3: (*Used to control the modem -CD signal in the loop-back mode.)
Logic 0 = Forces INT (A-D) outputs to the three state mode during the 16 mode. (normal default condition) In the Loop-back mode, sets -OP2 (-CD) internally to a logic 1.
Logic 1 = Forces the INT (A-D) outputs to the active mode during the 16 mode. In the Loop-back mode, sets -OP2 (-CD) internally to a logic 0.

MCR BIT-4:
Logic 0 = Disable loop-back mode. (normal default condition)
Logic 1 = Enable local loop-back mode (diagnostics).

MCR BIT 5-7:
Not used - Initialized to a logic 0.

Line Status Register (LSR)

This register provides the status of data transfers between the 454 and the CPU.

LSR BIT-0:
Logic 0 = No data in receive holding register. (normal default condition)
Logic 1 = Data has been received and is saved in the receive holding register.

LSR BIT-1:
Logic 0 = No overrun error. (normal default condition)
Logic 1 = Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the RHR is full. In this case the previous data in the shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the RHR, therefore the data in the RHR is not corrupted by the error.

LSR BIT-2:
Logic 0 = No parity error. (normal default condition)
Logic 1 = Parity error. The receive character does not have correct parity information and is suspect. In the RHR mode, this error is associated with the character

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at the top of the RHR.

LSR BIT-3:
Logic 0 = No framing error. (normal default condition)
Logic 1 = Framing error. The receive character did not have a valid stop bit(s).

LSR BIT-4:
Logic 0 = No break condition. (normal default condition)
Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time).

LSR BIT-5:
This bit indicates that the 454 is ready to accept new characters for transmission. This bit causes the 454 to issue an interrupt to the CPU when the transmit holding register is empty and the interrupt enable is set.

Logic 0 = Transmit holding register is not empty. (normal default condition)
Logic 1 = Transmit holding register is empty.

LSR BIT-6:
Logic 0 = Transmitter holding and shift registers are full.
Logic 1 = Transmitter holding and shift registers are empty (normal default condition).

LSR BIT-7:
Not used - Initialized to a logic 0.

Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device that the 454 is connected to. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

MSR BIT-0:
Logic 0 = No -CTS Change (normal default condition)
Logic 1 = The -CTS input to the 454 has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-1:
Logic 0 = No -DSR Change. (normal default condition)
Logic 1 = The -DSR input to the 454 has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-2:
Logic 0 = No -RI Change. (normal default condition)
Logic 1 = The -RI input to the 454 has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.

MSR BIT-3:
Logic 0 = No -CD Change. (normal default condition)
Logic 1 = Indicates that the -CD input to the has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-4:
-CTS (active high, logical 1). Normally MSR bit-4 bit is the compliment of the -CTS input. However in the loop-back mode, this bit is equivalent to the RTS bit in the MCR register.

MSR BIT-5:
DSR (active high, logical 1). Normally this bit is the compliment of the -DSR input. In the loop-back mode, this bit is equivalent to the DTR bit in the MCR register.

MSR BIT-6:
RI (active high, logical 1). Normally this bit is the compliment of the -RI input. In the loop-back mode this bit is equivalent to the OP1 bit in the MCR register.

MSR BIT-7:
CD (active high, logical 1). Normally this bit is the compliment of the -CD input. In the loop-back mode this bit is equivalent to the OP2 bit in the MCR register.

Scratchpad Register (SPR)

The ST16C454 provides a temporary data register to store 8 bits of user information.

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ST16C454 EXTERNAL RESET CONDITIONS

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7= input signals

SIGNALS	RESET STATE
TX A-D	High
-RTS A-D	High
-DTR A-D	High
INT A-D	Three-State

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AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T_{1w},T_{2w}	Clock pulse duration	17		17		ns	
T_{3w}	Oscillator/Clock frequency		8		24	MHz	
T_{6s}	Address setup time	5		0		ns	
T_{7d}	-IOR delay from chip select	10		10		ns	
T_{7w}	-IOR strobe width	35		25		ns	
T_{7h}	Chip select hold time from -IOR	0		0		ns	
T_{9d}	Read cycle delay	40		30		ns	
T_{12d}	Delay from -IOR to data		35		25	ns	
T_{12h}	Data disable time		25	35	15	ns	
T_{13d}	-IOW delay from chip select	10		10		ns	
T_{13w}	-IOW strobe width	35		25		ns	
T_{13h}	Chip select hold time from -IOW	0		0		ns	
T_{15d}	Write cycle delay	40		30		ns	
T_{16s}	Data setup time	20		15		ns	
T_{16h}	Data hold time	5		5		ns	
T_{17d}	Delay from -IOW to output		50		40	ns	100 pF load
T_{18d}	Delay to set interrupt from MODEM input		40		35	ns	100 pF load
T_{19d}	Delay to reset interrupt from -IOR		40		35	ns	100 pF load
T_{20d}	Delay from stop to set interrupt		1		1	Rclk	
T_{21d}	Delay from -IOR to reset interrupt		45		40	ns	100 pF load
T_{22d}	Delay from stop to interrupt		45		40	ns	
T_{23d}	Delay from initial INT reset to transmit start	8	24	8	24	Rclk	
T_{24d}	Delay from -IOW to reset interrupt		45		40	ns	
T_{25d}	Delay from stop to set -RxRdy		1		1	Rclk	
T_{26d}	Delay from -IOR to reset -RxRdy		45		40	ns	
T_{27d}	Delay from -IOW to set -TxRdy		45		40	ns	
T_{28d}	Delay from start to reset -TxRdy		8		8	Rclk	
T_{30s}	Address setup time	10		10		ns	
T_{30w}	Chip select strobe width	40		40		ns	
T_{30h}	Address hold time	15		15		ns	
T_{30d}	Read cycle delay	70		70		ns	
T_{31d}	Delay from -CS to data	15		15		ns	
T_{31h}	Data disable time			15		ns	
T_{32s}	Write strobe setup time	10		10		ns	
T_{32h}	Write strobe hold time	10		10		ns	
T_{32d}	Write cycle delay	70		70		ns	

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Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T_{33s}	Data setup time	20		15		ns	
T_{33h}	Data hold time	10		10		ns	
T_R	Reset pulse width	40		40		ns	
N	Baud rate devisor	1	2^{16}-1	1	2^{16}-1	Rclk	

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ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND - 0.3 V to VCC +0.3 V
Operating temperature	-40° C to +85° C
Storage temperature	-65° C to 150° C
Package dissipation	500 mW

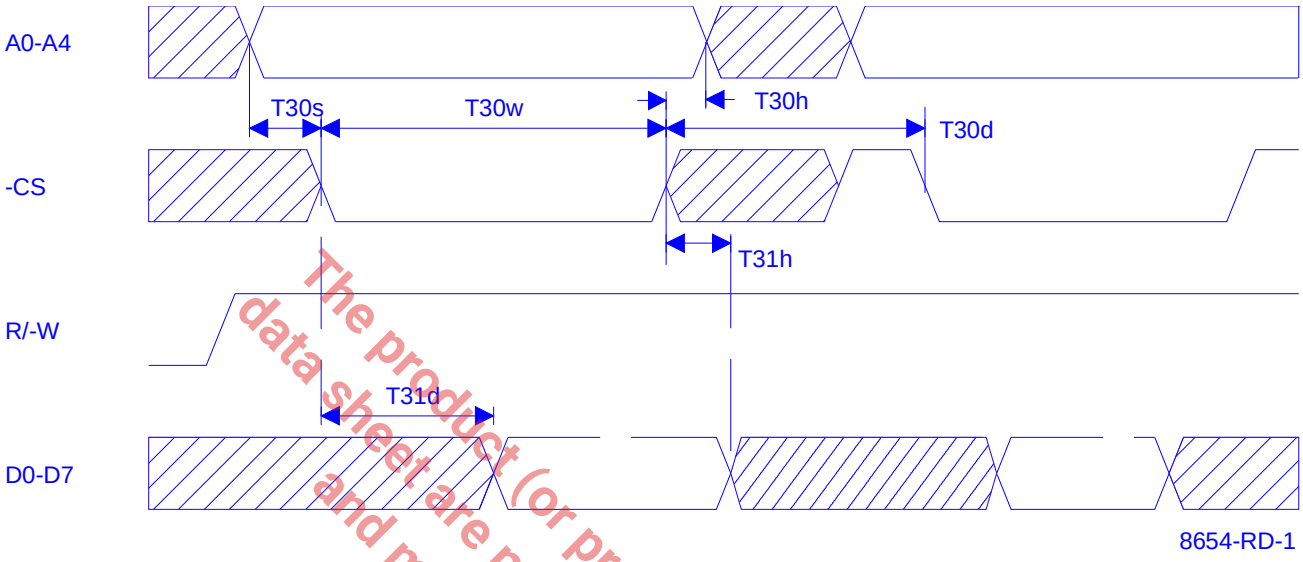
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

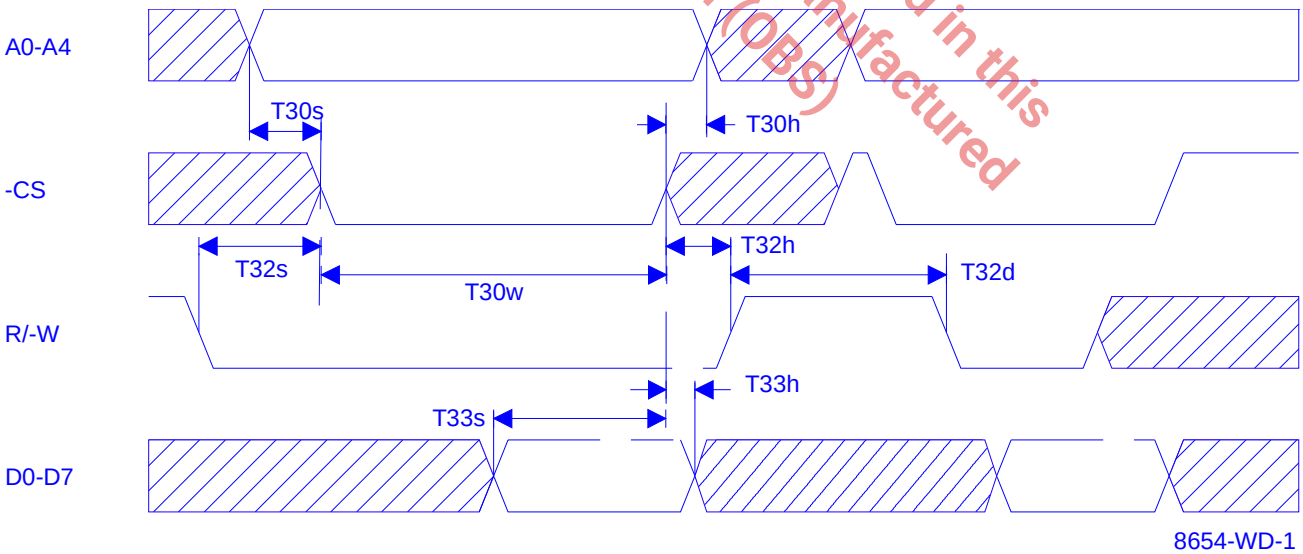
Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
V_{ILCK}	Clock input low level	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock input high level	2.4	VCC	3.0	VCC	V	
V_{IL}	Input low level	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input high level	2.0		2.2	VCC	V	
V_{OL}	Output low level on all outputs				0.4	V	I_{OL}= 5 mA
V_{OL}	Output low level on all outputs		0.4			V	I_{OL}= 4 mA
V_{OH}	Output high level			2.4		V	I_{OH}= -5 mA
V_{OH}	Output high level	2.0				V	I_{OH}= -1 mA
I_{IL}	Input leakage		±10		±10	µA	
I_{CL}	Clock leakage		±10		±10	µA	
I_{CC}	Avg power supply current		3		6	mA	
C_P	Input capacitance		5		5	pF	
R_{IN}	Internal pull-up resistance	3			15	kΩ	

Note: See the Symbol Description Table, for a listing of pins having internal pull-up resistors.

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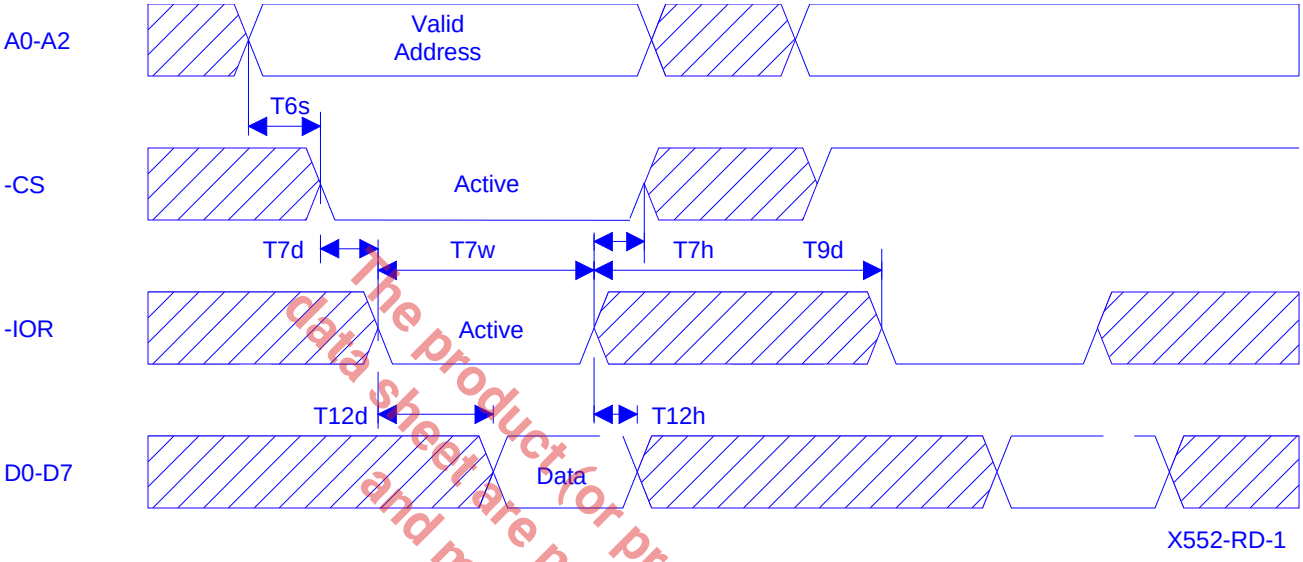


General read timing in 68 mode

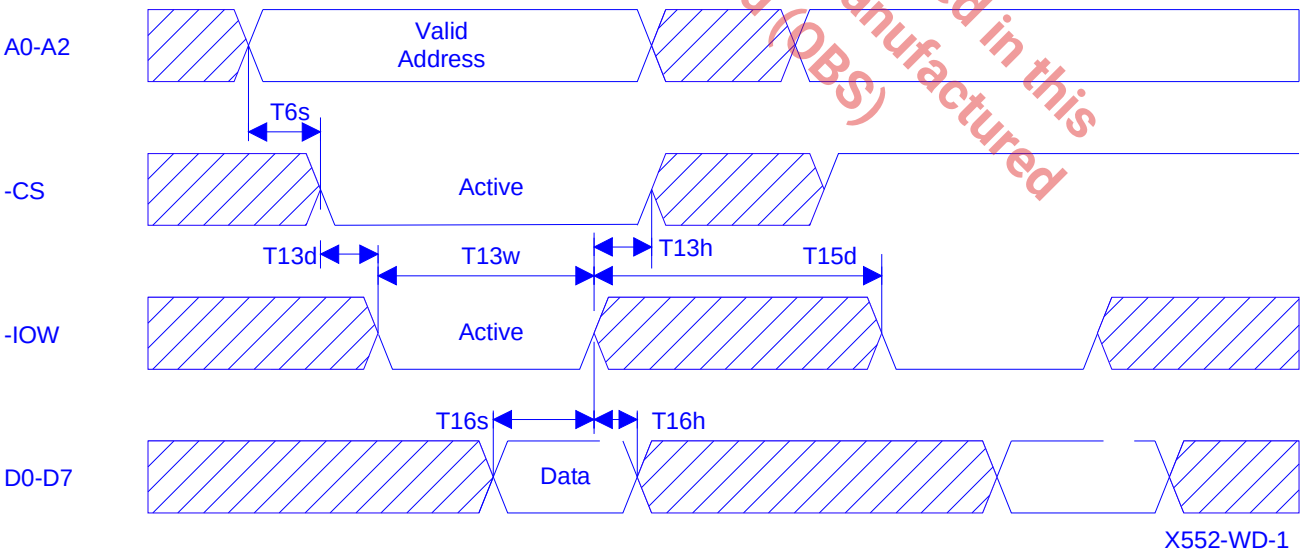


General write timing in 68 mode

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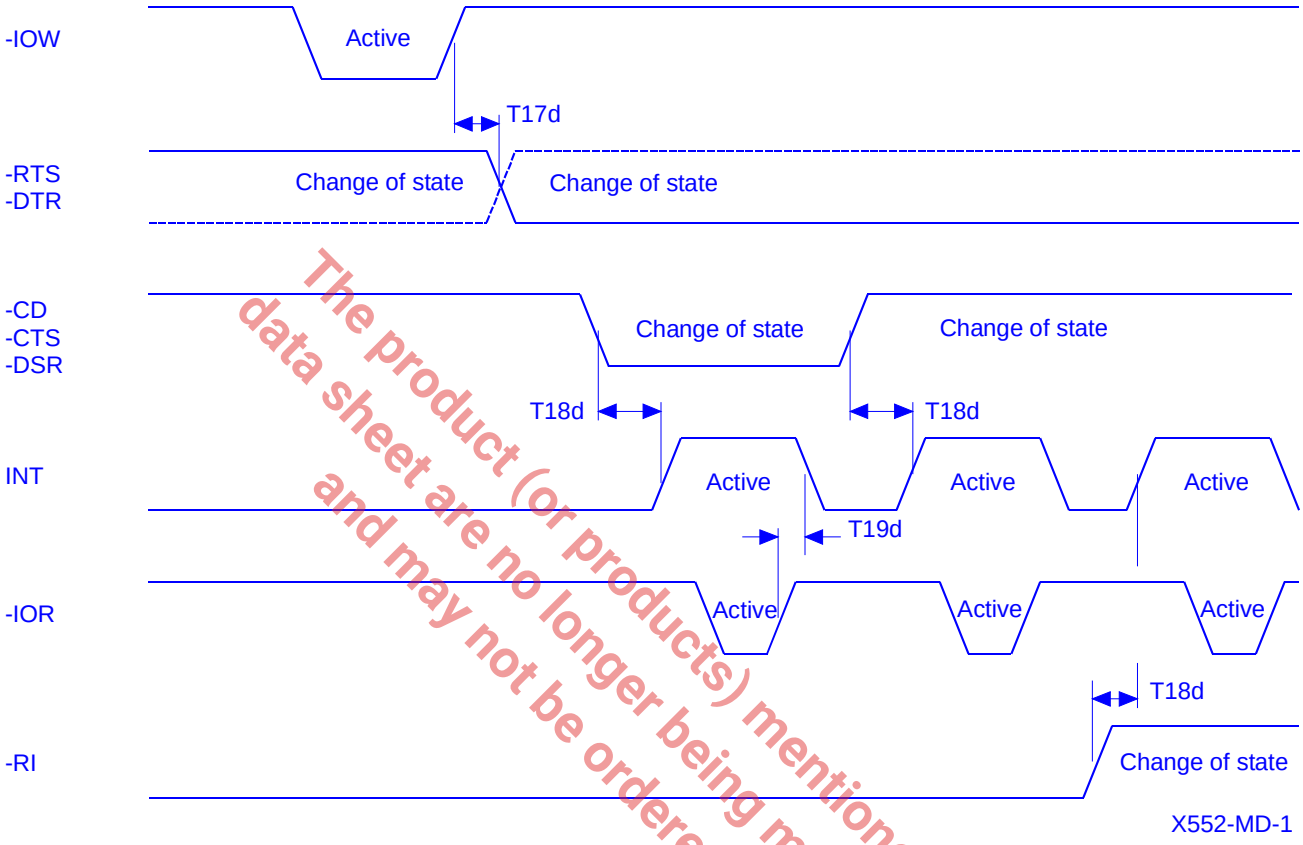


General read timing in 16 mode

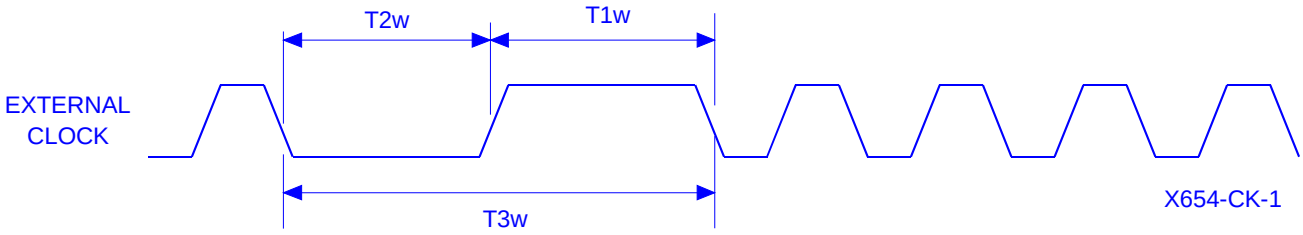


General write timing in 16 mode

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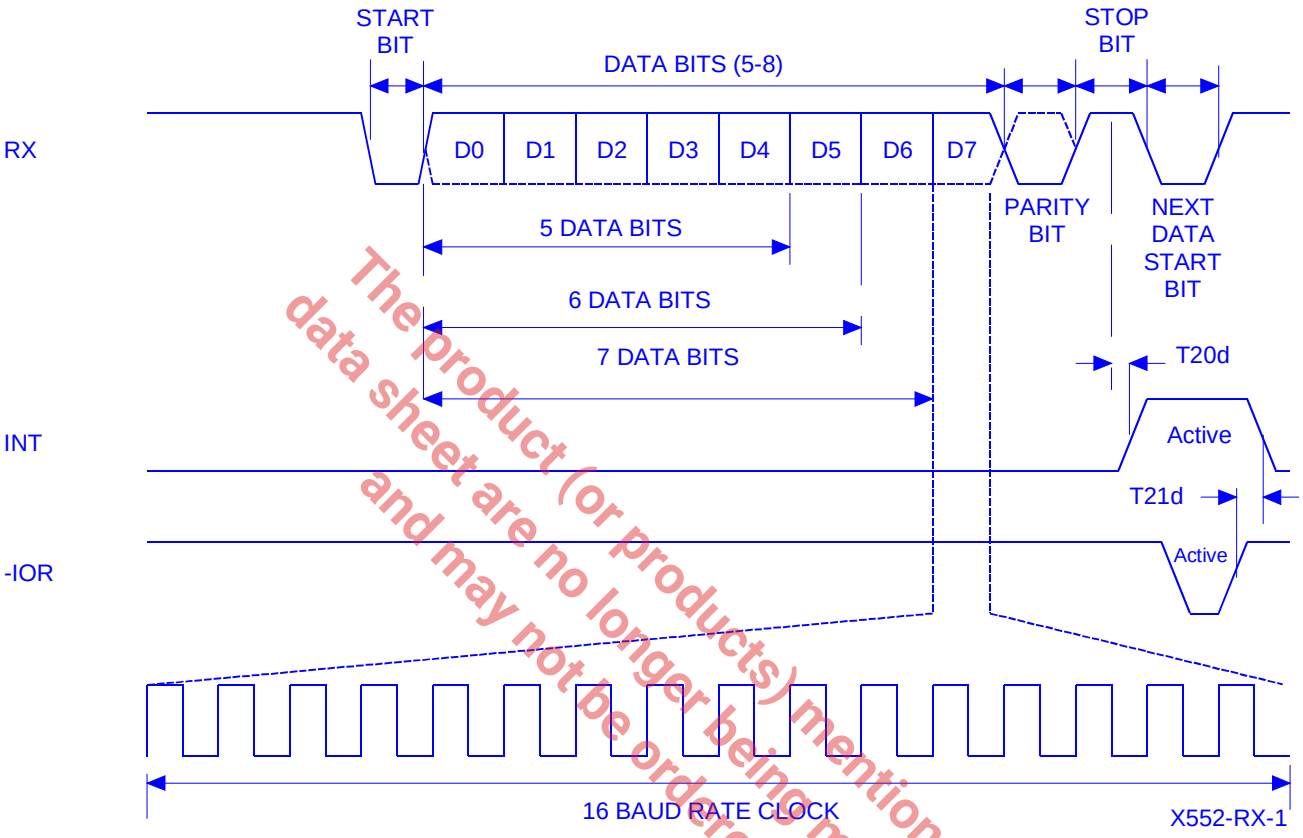


Modem input/output timing



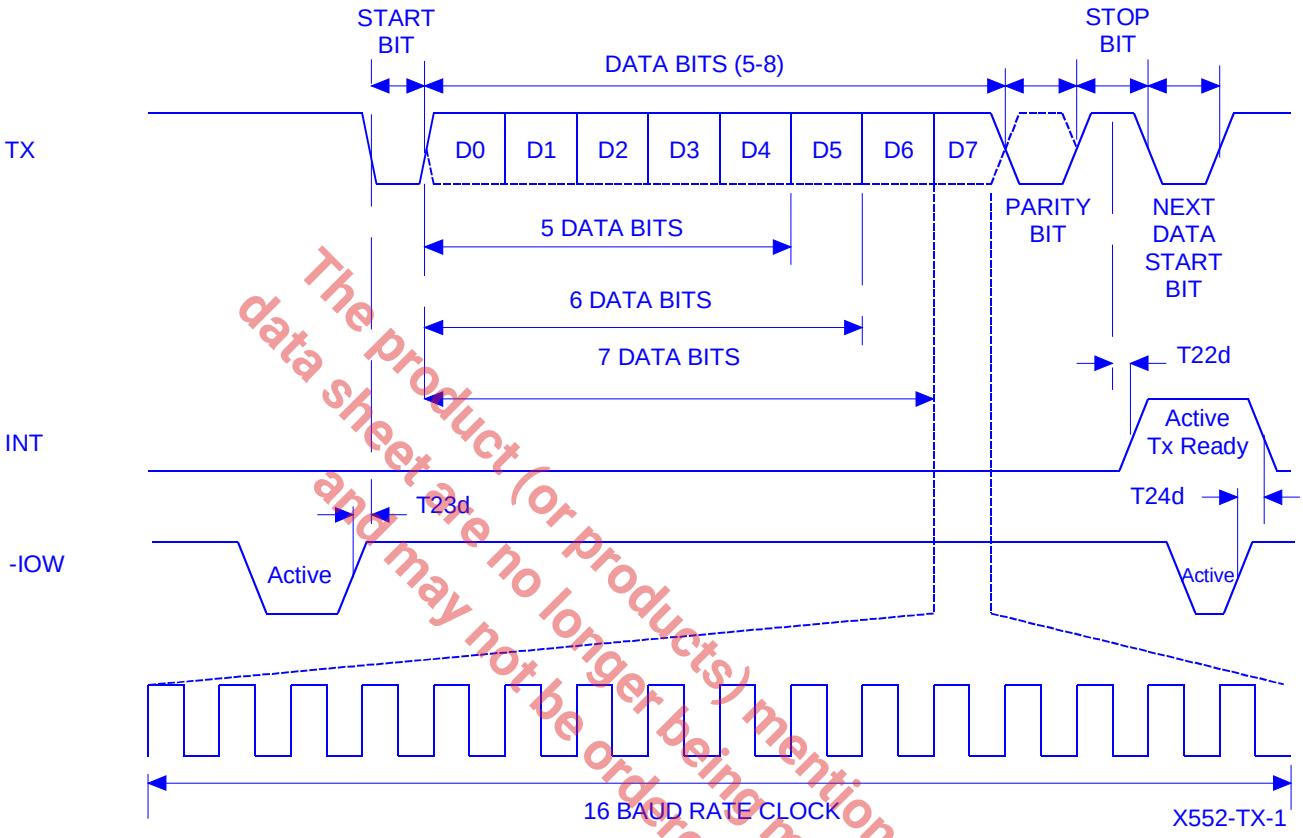
External clock timing

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Receive timing

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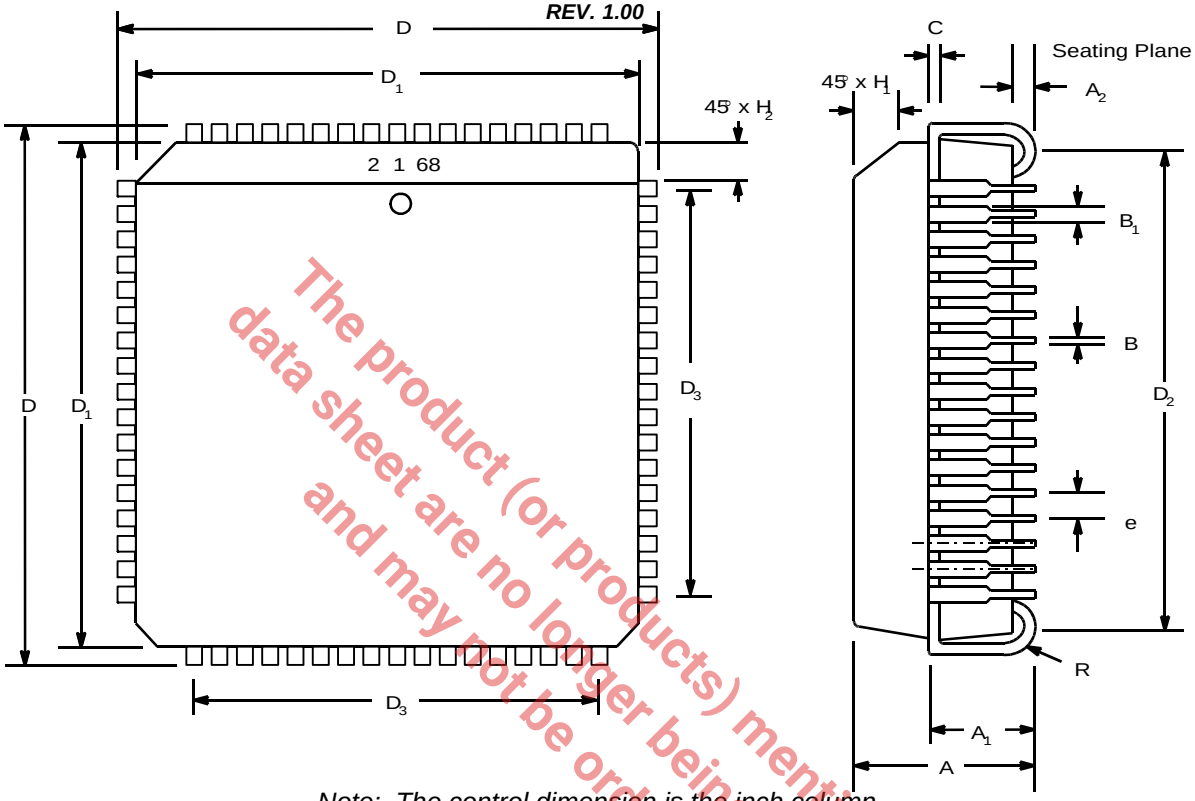


Transmit timing

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68 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

REV. 1.00



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Note: The control dimension is the inch column.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.200	4.19	5.08
A_1	0.090	0.130	2.29	3.30
A_2	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.985	0.995	25.02	25.27
D_1	0.950	0.958	24.13	24.33
D_2	0.890	0.930	22.61	23.62
D_3	0.800 typ		20.32 typ	
e	0.050 BSC		1.27 BSC	
H_1	0.042	0.056	1.07	1.42
H_2	0.042	0.048	1.07	1.22
R	0.25	0.045	0.64	1.14

EXPLANATION OF DATA SHEET REVISIONS:

FROM	TO	CHANGES	DATE
3.20	3.30	Added revision history. Added Device Status to front page.	August 2004
3.30	3.31	Removed discontinued ST68C454 from Ordering Information.	August 2005

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