88LX2720

Data Sheet
Wave-2 G.hn AFE

General Description

This data sheet describes MaxLinear's 88LX2720 Wave-2 G.hn AFE.

The 88LX2720 is a programmable, high-performance Wave-2 G.hn AFE for powerline communications with a single transmission channel and two reception channels to enable both SISO operation using one device and MIMO using two devices. In addition to the transmission and reception paths, the 88LX2720 contains a biasing circuit and a register block controlled from the digital interface.

Applications

- Powerline-to-Ethernet adapter.
- WiFi extender.
- Embedded G.hn modem.

Features

- Designed for powerline, baseband coaxial and phone line wiring.
- Programmable transmission and reception gains.
- Integrated filters.
- Integrated line drivers.
- Power down and standby mode.
- Very low noise and distortion over the entire transmission and reception paths.
- 28 pin QFN 4×4mm package.
- Support for multiple AFEs operating in parallel with only one digital baseband (DBB) processor 88LX5152.

Supported Standards

- Code of Conduct on Energy Consumption of Broadband Equipment Version 5.0, European Commission.
- ITU-T G.9960: Unified high-speed wireline-based home networking transceivers – System architecture and physical layer specification *(*referenced as ITU-T G.9960*).*
- ITU-T G.9961: Unified high-speed wire-line based home networking transceivers – Data link layer specification *(*referenced as ITU-T G.9961*).*
- ITU-G.9962: Unified high-speed wire-line based home networking transceivers – Management specification *(*referenced as ITU-T G.9962*).*
- ITU-T G.9963: Unified high-speed wireline-based home networking transceivers – Multiple input/multiple output specification *(*referenced as ITU-T G.9963*).*
- ITU-T G.9964: Unified high-speed wire-line based home networking transceivers - Power spectral density specification *(*referenced as ITU-T G.9964).

Revision History

Document No.	Release Date	Change Description
073-2720DSR03	July 14, 2020	**Updated:** ■ Confidentiality protection removed. ■ New template applied.
056DSR02	July 18, 2017	Initial release.

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Introduction

The 88LX2720 is a programmable, high-performance Wave-2 G.hn AFE powerline communications with a single transmission channel and two reception channels to enable both SISO operation using one device and MIMO using two. In addition to the transmission and reception paths, the 88LX2720 contains a biasing circuit and a register block controlled from the digital interface.

Transmission path comprises a programmable transimpedance amplifier, a filter, and two line drivers to condition and amplify the OFDM signal from the DAC up to a level suitable for the wireline. Each reception path comprises an attenuator, a LNA, a filter, and a PGA to accommodate the signal from the wireline to a level suitable for the ADC range.

The operating mode of the 88LX2720 is highly configurable to balance performance and power consumption based on the requirements of bandwidth, power density, and physical medium.

The biasing block uses a bandgap reference generator adjusted with an external resistor to generate the biasing current and voltage for all the blocks of the circuit.

The digital interface is used to configure the register set from the baseband transceiver.

The 88LX2720 is supplied from 5V and 3.3V.

IC Block Diagram

The following figure shows the functional block diagram of the 88LX2720.

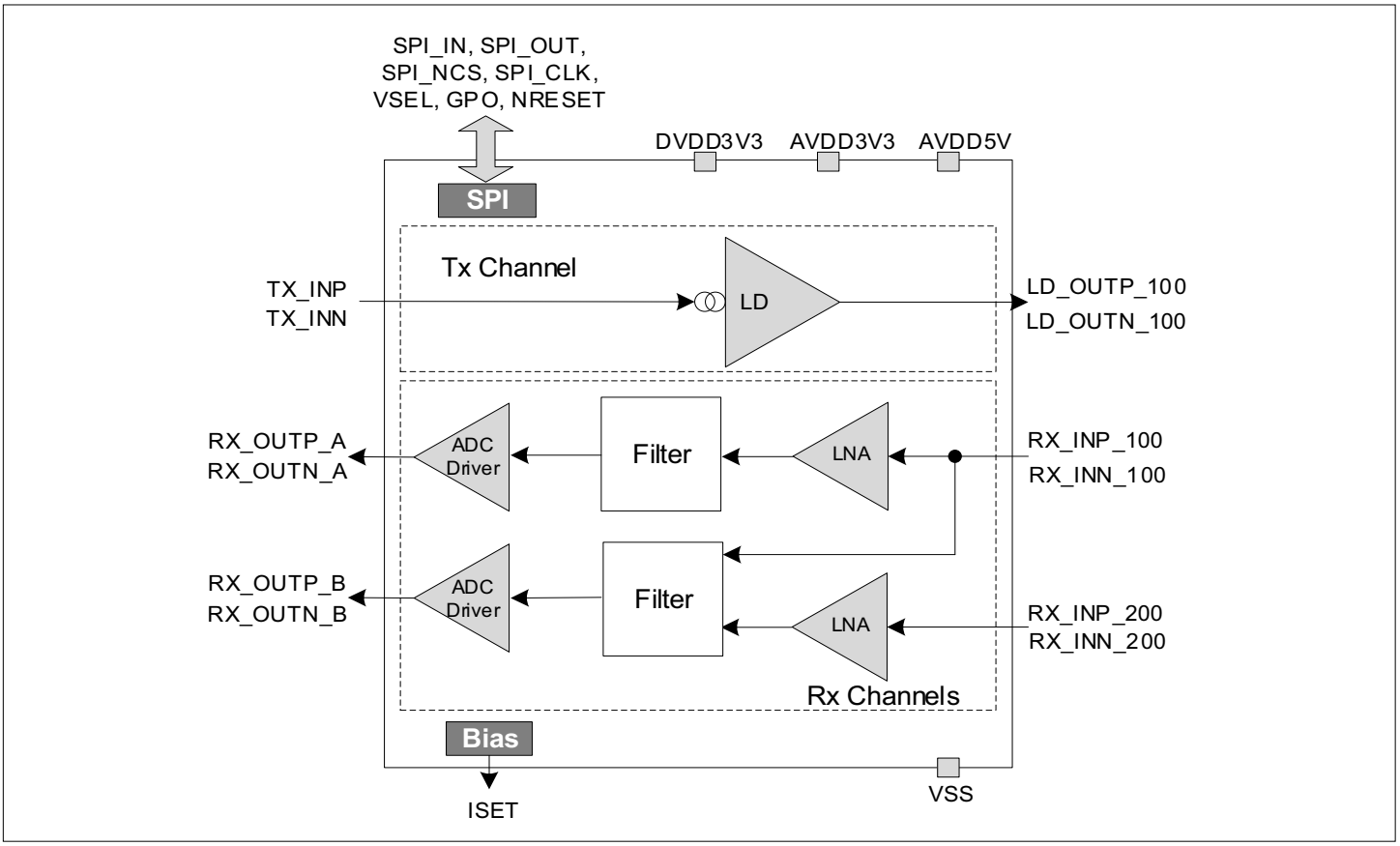

Figure 1: 88LX2720 Block Diagram

Typical Application

The Wave-2 G.hn chipset (88LX5152 and 88LX2720) can be used in stand-alone or embedded applications. The typical applications are listed in the following subsections

Powerline-to-Ethernet Adapter

The powerline-to-Ethernet adapter is a standalone application containing the Wave-2 G.hn chipset (88LX5152 and 88LX2720), power supply, and Gigabit Ethernet interface in a single wall-plug box. MaxLinear provides reference designs implementing this application including Gigabit Ethernet and PLC MIMO modes, in which two 88LX2720 devices are used. This design can also be modified to use SISO only. In this case, only one 88LX2720 device is needed.

The following figure shows the block diagram of the powerline-to-Ethernet MIMO implementation.

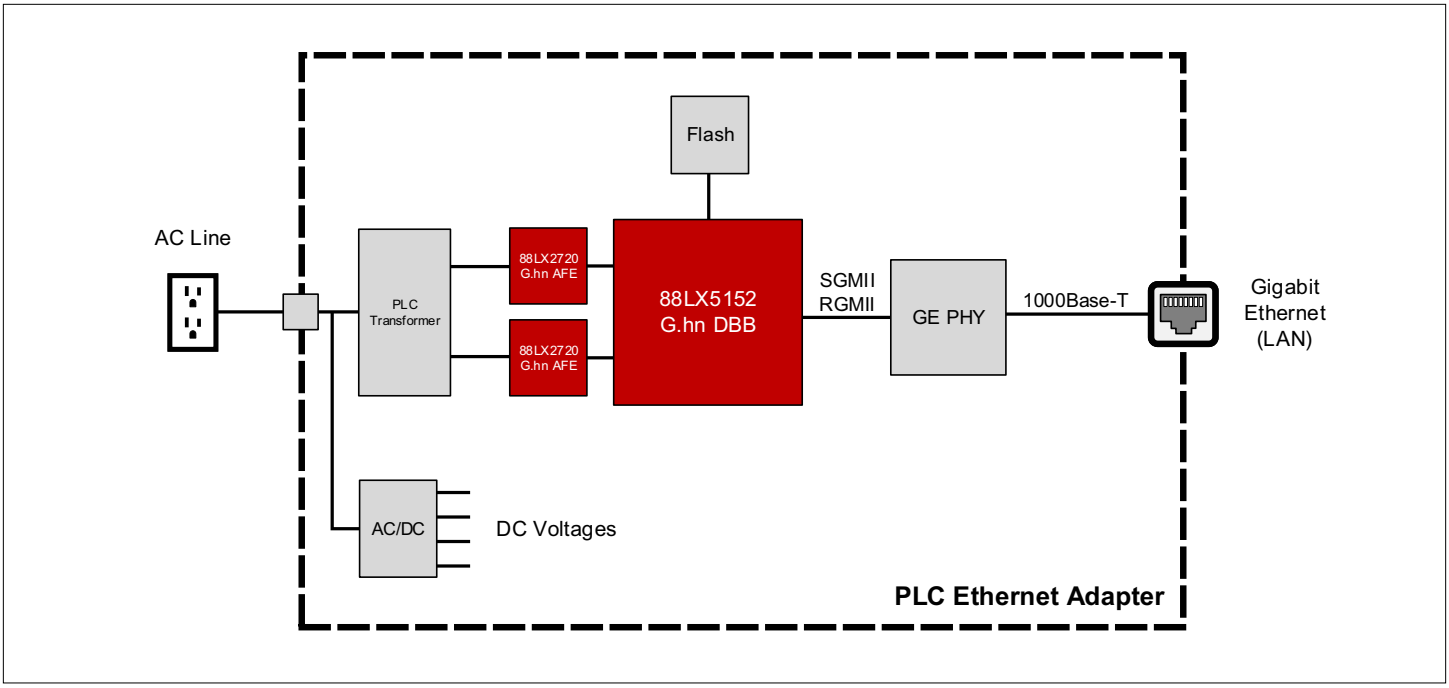

Figure 2: G.hn Gigabit Ethernet MIMO PLC Adapter Block Diagram

The following figure shows the block diagram of a SISO implementation.

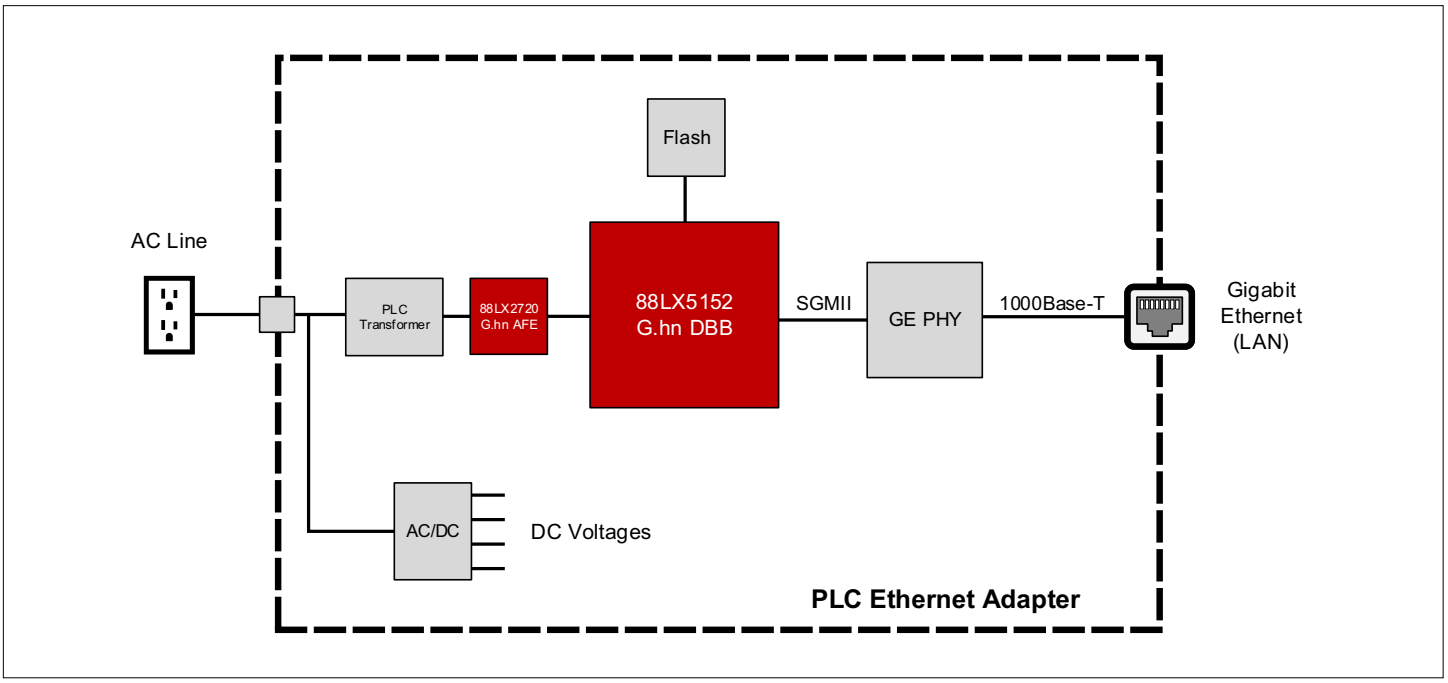

Figure 3: G.hn Gigabit Ethernet SISO PLC Adapter Block Diagram

WiFi Extender

The powerline-WiFi extender is a stand-alone application containing the G.hn chipset, a CPU, the power supply, and a WiFi access point in a single platform which is used to improve the coverage of wireless networks when the distance from a primary access point does not allow for an acceptable performance with the wireless end point. Placing this device including a secondary access point nearer the end point using power line as backbone provides significant improvement in this wireless link.

This application can implement Gigabit Ethernet interface, PLC MIMO, and any kind of *IEEE 802.11* based WiFi access point. The design can be modified to use SISO only as well as to provide the backbone over coaxial or phone lines.

The following figure shows the block diagram of the powerline-WiFi platform example.

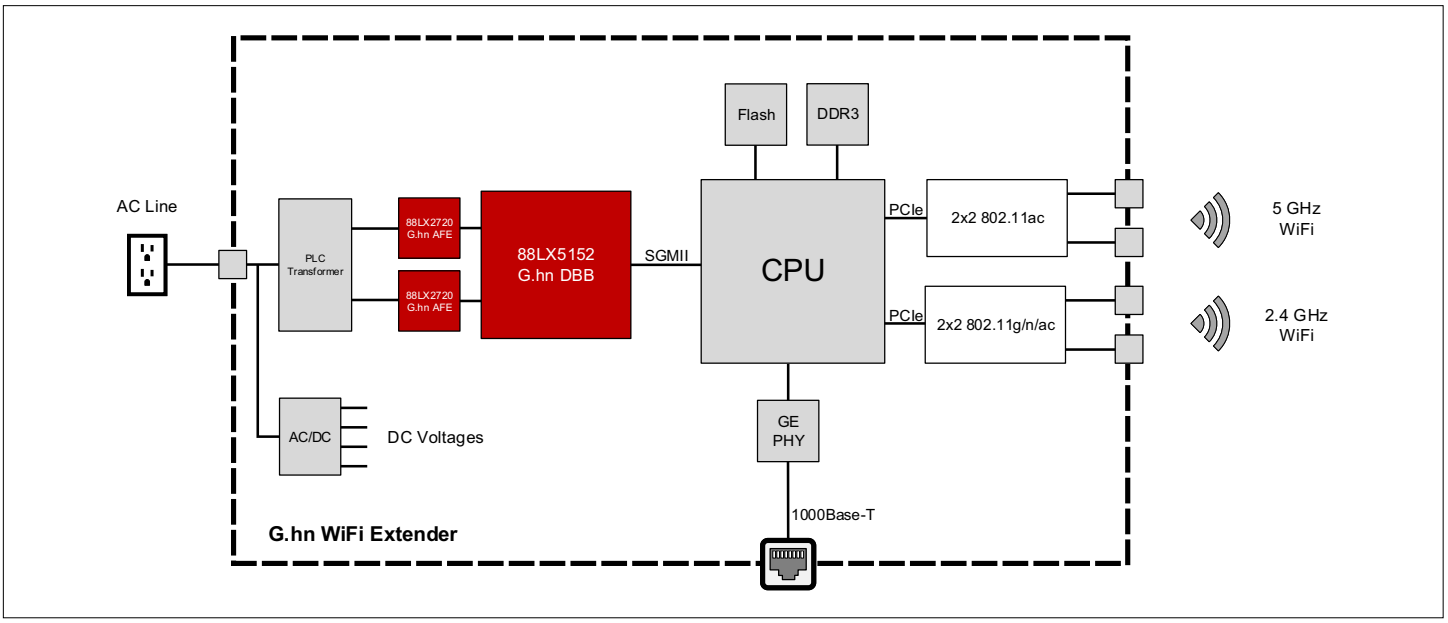

Figure 4: Powerline-WiFi Extender Block Diagram

Embedded G.hn Modem

The G.hn chipset can be embedded in other designs to provide a powerful networking capability on wired media other than Ethernet.

The following figure shows the block diagram of an embedded G.hn modem. As for Ethernet adapters and WiFi extenders, both SISO and MIMO configurations are supported.

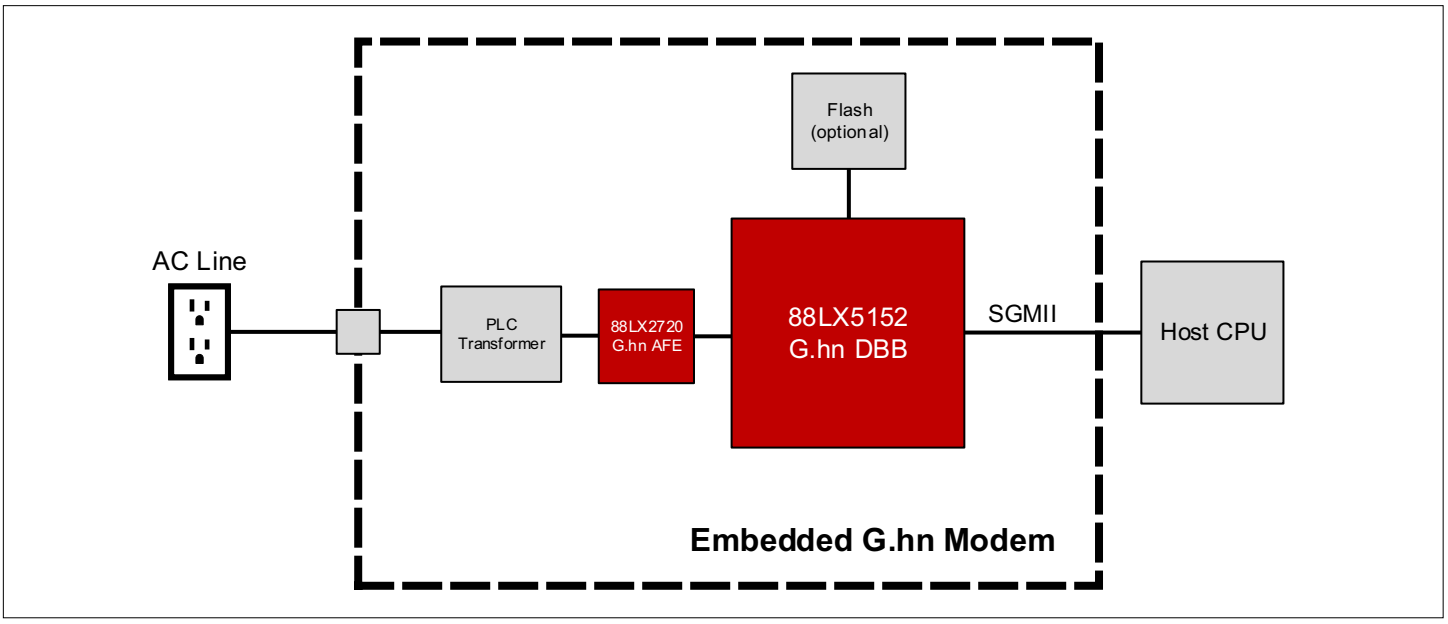

Figure 5: Embedded G.hn Modem Block Diagram

Pin Information

Pin Configuration

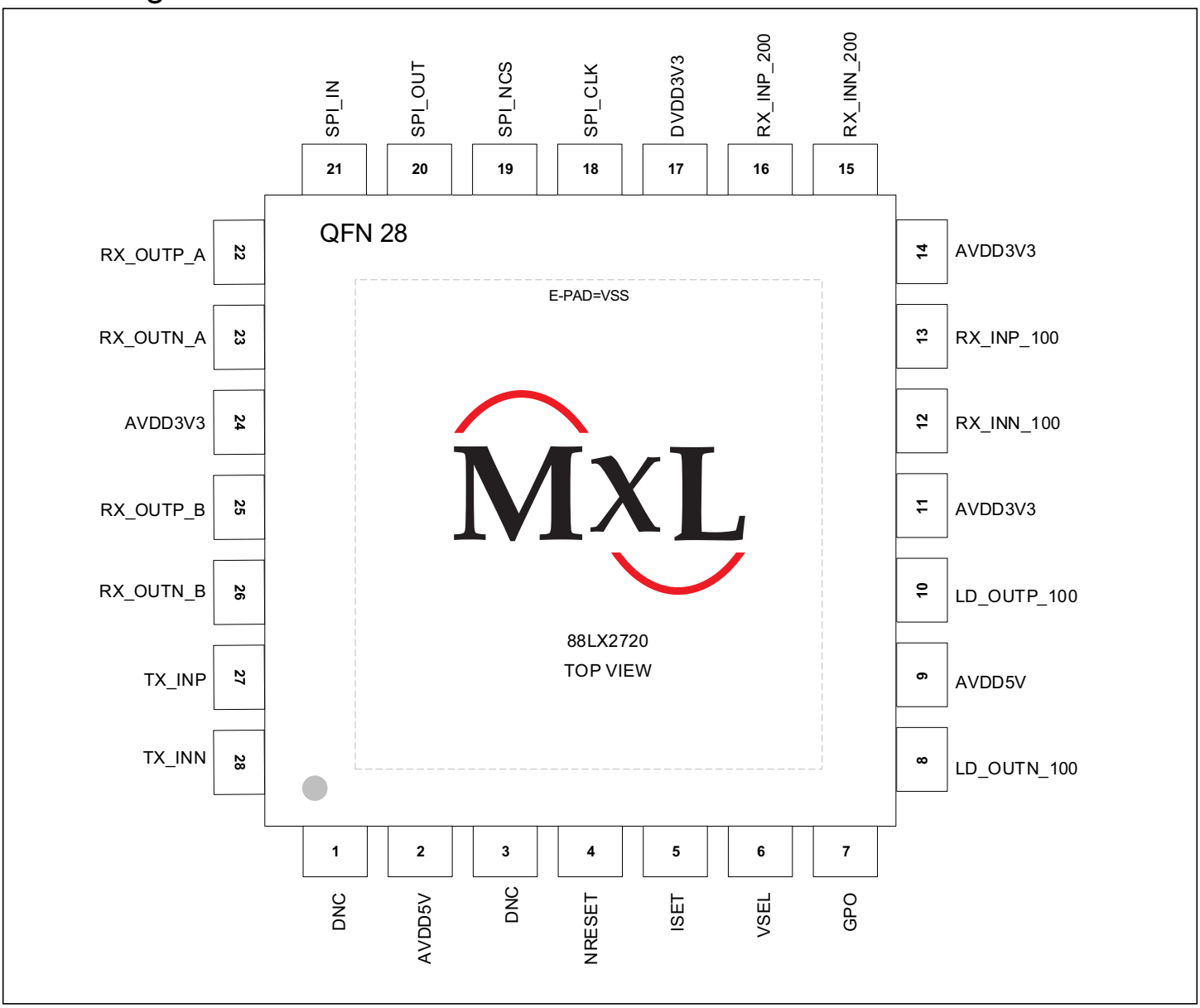

Figure 6: 88LX2720 Package Pinout

Pin Description

The following table lists pins and signal names. Power pins are also listed in this table.

Table 1: 88LX2720 Pin Description

Pin #	Pin Name	Type	Description
11, 14, 24	AVDD3V3	PWR	Analog 3.3V supply.
2, 9	AVDD5V	PWR	Analog 5V supply.
1, 3	DNC	-	Do Not Connect.
17	DVDD3V3	PWR	Digital 3.3V supply.
7	GPO	DO	General Purpose Output.
5	ISET	AO	Biasing resistor (6kΩ 1% accuracy connected to ground).
8	LD_OUTN_100	AO	Tx 100 negative output.
10	LD_OUTP_100	AO	Tx 100 positive output.
4	NRESET	DI	SPI Reset (active low).
12	RX_INN_100	AI	Rx 100 negative input.
15	RX_INN_200	AI	Rx 200 negative input.
13	RX_INP_100	AI	Rx 100 positive input.
16	RX_INP_200	AI	Rx 200 positive input.
23	RX_OUTN_A	AO	Rx A negative output.
26	RX_OUTN_B	AO	Rx B negative output.
22	RX_OUTP_A	AO	Rx A positive output.
25	RX_OUTP_B	AO	Rx B positive output.
18	SPI_CLK	DI	SPI Clock.
21	SPI_IN	DI	SPI Data input.
19	SPI_NCS	DI	SPI Chip Select (active low).
20	SPI_OUT	DI/DO	SPI Data output.
28	TX_INN	AI	Tx negative input.
27	TX_INP	AI	Tx positive input.
6	VSEL	AI	IC selector in multi AFE uses cases.
Exposed Pad	VSS	GND	Ground.

Signal Description

Table 2: Signal Types

Pin Name	Description
AI	Analog Input.
AO	Analog Output.
DI	Digital Input.
DO	Digital Output.
DI/DO	Digital input/Digital Output.
GND	Ground.
PWR	Power Supply.

Electrical Specifications

Absolute Maximum Ratings

Important: The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability. Solder reflow profile is specified in the *IPC/JEDEC J-STD-020C* standard.

Table 3: Absolute Maximum Ratings

Parameter	Maximum	Units
AVDD5V to VSS	From –0.3 to 6.0	V
AVDD3V3, DVDD3V3 to VSS	From –0.3 to 4.0	V
LD_OUTN_100, LD_OUTP_100, RX_INN_100, RX_INP_100, RX_INN_200, RX_INP_200, VSEL to VSS	–0.3 to AVDD5V + 0.3	V
NRESET, ISET, GPO, SPI_CLK, SPI_NCS, SPI_OUT, SPI_IN, RX_OUTP_A, RX_OUTN_A, RX_OUTP_B, RX_OUTN_B to VSS	From –0.3 to AVDD3V3 + 0.3	V
TX_INP, TX_INN to VSS	From –0.3 to 1.95	V
ESD susceptibility at all pins, HBM	2	kV
Maximum Junction Temperature	150	°C
Storage Temperature Range	From –65 to 150	°C

Required Operating Conditions

Table 4: Required Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{AVDD5V}	Analog Supply Voltage AVDD5V	4.75	5	5.5	V
$V_{AVDD3V3}$	Analog Supply Voltage AVDD3V3	3.135	3.3	3.465	V
$V_{DVDD3V3}$	Digital Supply Voltage DVDD3V3	3.135	3.3	3.465	V
T_A	Ambient Operating Temperature (Commercial Grade)	0	-	70	°C
T_{JMAX}	Maximum Operational Junction Temperature	-	-	125	°C

Electrical Characteristics

Note: Power consumption figures depend on the configuration programmed in the firmware. The values listed in this section correspond to the optimal AFE configuration at the time of qualifying the silicon.

The following figures, unless otherwise stated, are measured at T_A = –40..85°C, AVDD3V3 = 3.3V±5%, DVDD3V3 = 3.3V±5%, AVDD5V = 4.75..5.5V. Typical values are at T_A = 25°C, AVDD3V3 = 3.3V, DVDD3V3 = 3.3V, AVDD5V = 5V, unless otherwise noted. Biasing setup configured as nominal value.

Specifications over the operating temperature range are assured by design, characterization and correlation with statistical process controls.

Table 5: Power Node Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
General, all the IC						
I_{AVDD5V}	Total Quiescent Current at AVDD5V	V(NRESET)=0	-	0.7	-	mA
		V(NRESET)=AVDD3V3	-	3.8	-	
$I_{AVDD3V3}$	Total Quiescent Current at AVDD3V3	V(NRESET)=0	-	0.3	-	mA
		V(NRESET)=AVDD3V3	-	0.7	-	
$I_{DVDD3V3}$	Total Quiescent Current at DVDD3V3	V(NRESET)=0	-	0.1		mA
		V(NRESET)=AVDD3V3	-	0.2	-	

Table 6: Transmission Mode

Symbol	Symbol	Conditions	Minimum	Typical	Maximum	Units
I_{AVDD5V}	Total Current at AVDD5V	Output signal: 16.5dBm over 100Ω load through 1:3 transformer.	-	130	-	mA
$I_{AVDD3V3}$	Total Current at AVDD3V3	Output signal: 16.5dBm over 100Ω load through 1:3 transformer.	-	50	-	mA
R_F	Programmable Differential Transimpedance	-	-	1783 1416 1125 893 710 563	-	Ω
ΔR_F	Gain Step	R_F = 563–1783	-	2	-	dB
f_c	–3dB Bandwidth	R_F = 563 to 1783 Small Signal Bandwidth Load=Powerline	100	-	-	MHz
I_{INdiff}	Recommended Differential Input Current Range	-	-	5	-	mApp

Table 7: Receptions Mode, per Channel

Symbol	Symbol	Conditions	Minimum	Typical	Maximum	Units
I_{AVDD5V}	Total Current at AVDD5V	-	-	5	-	mA
$I_{AVDD3V3}$	Total Current at AVDD3V3	-	-	227	-	mA
ΔG	Gain Step	G= –26dB to + 30dB	-	2	-	dB
f_c	–3dB Bandwidth	G= –26dB to + 30dB Small Signal Bandwidth Load=ADC	100	-	-	MHz
V_{INdiff}	Recommended Differential Input Current Range	-	0	-	2× AVDD5V	Vpp
$V_{OUTdiff}$	Recommended Differential Output Voltage Range	-	-	1.5	-	Vpp
R_{indiff}	Differential Input Resistance	Powerline mode G= –26dB to +30dB	-	1200	-	Ω

Table 8: Biasing

Symbol	Symbol	Conditions	Minimum	Typical	Maximum	Units
V_{ISET}	Voltage at ISET	External 6kΩ (1% accuracy) resistor connected to VSS	-	1.2	-	V
$Von_{AVDD3V3}$	Turn-On Threshold at AVDD3V3	Increasing AVDD3V3	-	-	2.85	V
$Voff_{AVDD3V3}$	Turn-Off Threshold at AVDD3V3	Decreasing AVDD3V3	2.5	-	-	V
$Vhys_{AVDD3V3}$	Hysteresis at AVDD3V3	-	-	130	-	mV
Von_{AVDD5V}	Turn-On Threshold at AVDD5V	Increasing AVDD5V	-		4.45	V
$Voff_{AVDD5V}$	Turn-Off Threshold at AVDD5V	Decreasing AVDD5V	3.9	-	-	V
$Vhys_{AVDD5V}$	Hysteresis at AVDD5V	-	-	350	-	mV
T_{OTS}	Over-Temperature Detector	High Threshold, increasing T_J	-	155	-	°C
		Low Threshold, decreasing T_J	-	115		
V_{INVSEL}	Recommended Input Voltage Range at VSEL pin. (See "Strapping Values" on page 15)	2b'11	-	AVDD5V	-	V
		2b'10	-	AVDD3V3	-	
		2b'01	-	1.5	-	
		2b'00	-	0	-	

Table 9: Digital Inputs and Outputs

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High Threshold at SPI_CLK, SPI_IN, SPI_NCS, NRESET	-	0.7×DVDD3V3	-	-	V
V_{IL}	Low Threshold at SPI_CLK, SPI_IN, SPI_NCS, NRESET	-	-	-	0.3× DVDD3V3	V
R_{PU}	Pull-Up Resistor at NRESET, SPI_NCS	-	-	70	-	KΩ
V_{OH}	Output High Level at SPI_OUT, GPO	I()=4mA	DVDD3V3-0.4	-	-	V
V_{OL}	Output Low Level at SPI_OUT, GPO	I()=4mA	-	-	0.4	V
$I_{LEAKAGE}$	Input Leakage Current at SPI_CLK, SPI_IN, SPI_NCS, SPI_OUT, NRESET, GPO	0 < V < DVDD3V3	-	-	10	µA

Digital Interface

The 88LX2720 includes a 4-wire serial interface similar to SPI. The operation of this interface and the mapping of the registers is specifically designed to work with 88LX5152 and 88LX5153, therefore the information provided in this section is only informative and not intended to explain the use of this device in stand-alone mode.

- Maximum clock frequency for write operations = 100MHz.
- Maximum clock frequency for read operations = 25MHz.
- Bit ordering within frames = MSB first.

The 88LX2720 supports two operating modes on the SPI interface:

- Single input mode = In this mode only the SPI_IN pin is used to send information to the AFE chip. The SPI_OUT pin remains in high impedance during write operations and outputs data during read operations. This mode is equivalent to the standard SPI mode 3 (CPOL=1, CPHA=1).

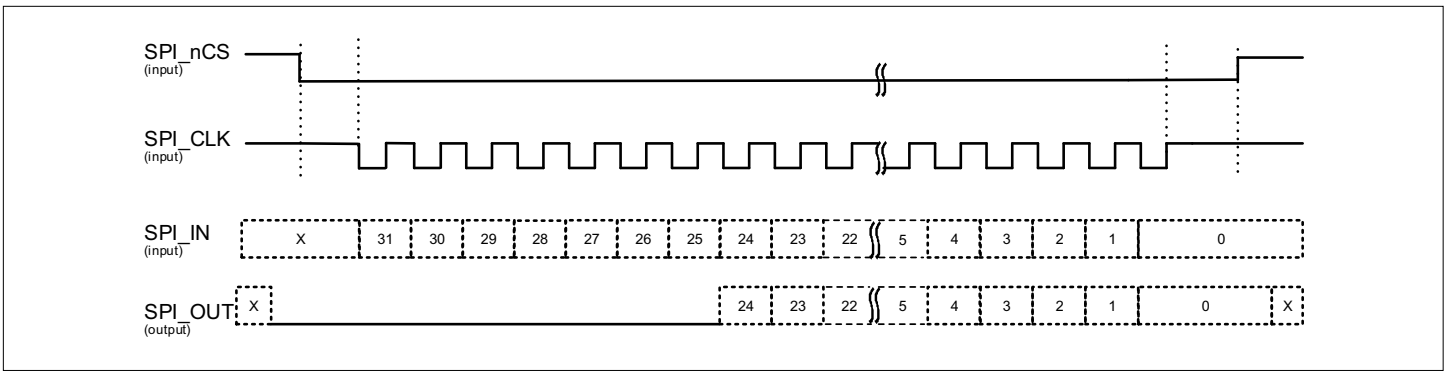

Figure 7: Single Input Mode

- Parallel input mode = In this mode the SPI_OUT pin becomes an input and works in parallel with SPI_IN, doubling the data rate and reducing the duration of the frame by half. The change to parallel input mode is configured in one of the registers during a previous single input transaction.

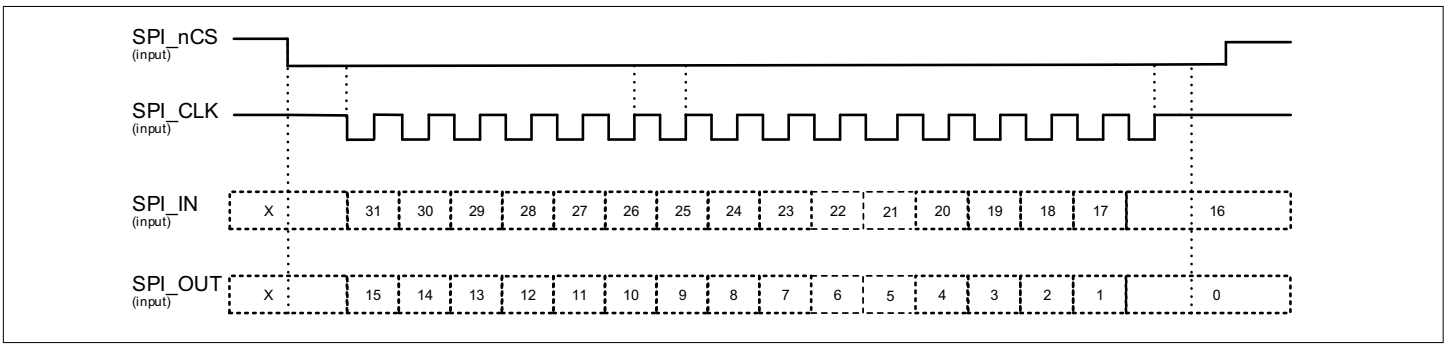

Figure 8: Parallel Input Mode

SPI_OUT remains in high impedance when SPI_NCS is not asserted. The biasing of the line is assured by the internal pull-up resistors of the AFE and the DBB devices.

When more than one AFE is used in a product, the SPI lines should be routed in a T shape with the branches reaching each device that has the same length.

Strapping Values

The 88LX2720 AFE may operate in multi-AFE systems comprising one 88LX5152 DBB processor and one or more AFE IC's all of them sharing a common SPI interface. To control each AFE IC separately a strapping value must be set externally to identify each AFE IC. This strapping value provides an internal identifier (2bits) for each AFE IC. This identifier must be used to compose the 6 bit address field of the SPI transaction.

Strapping is performed using VSEL pin which can be set to four different voltage values to define the device identifiers as listed in the following table.

Table 10: Strapping Values

VSEL pin (V)	VSEL field
0	2b'00
1.5	2b'01
3.3	2b'10
5	2b'11

Mechanical Drawings

28-Pin QFN Package

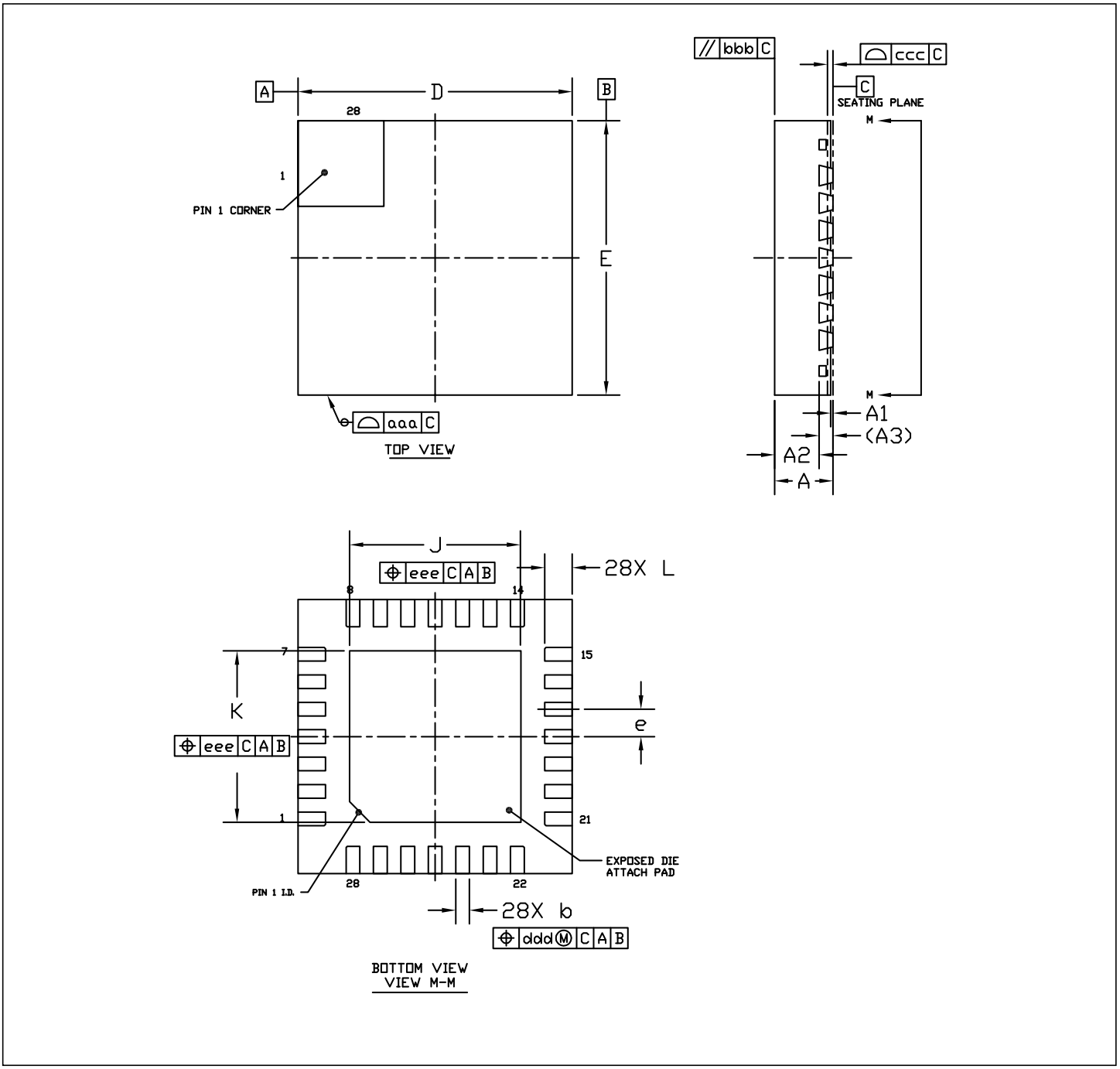

Figure 9: 28 QFN 4x4 Package Top and Lateral Views

Package Outline Parameters

Symbol	Parameter	Nominal	Maximum
A	0.80	0.85	0.90
A1	0	0.035	0.05
A2	-	0.65	0.67
A3	-	0.203 REF	-
b	0.15	0.20	0.25
D	-	4.0 BSC	-
E	-	4.0 BSC	-
e	-	0.40 BSC	-
J	2.4	2.5	2.6
K	2.4	2.5	2.6
L	0.35	0.40	0.45
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.08	-
ddd	-	0.10	-
eee	-	0.10	-

Note: All dimensions are in millimeters.

Table 11: Package Thermal Information

Symbol	Parameter	Minimum	Typical	Maximum	Unit
θ_{JC}	Thermal Resistance from Junction to the Top of the package	-	20.16	-	°C/W
θ_{JB}	Thermal Resistance from Junction to the Bottom of the package	-	19.45	-	°C/W

Ordering Information

Part Order Numbering

The following figure shows the part order numbering scheme for the 88LX2720. For more information, contact MaxLinear's technical support.

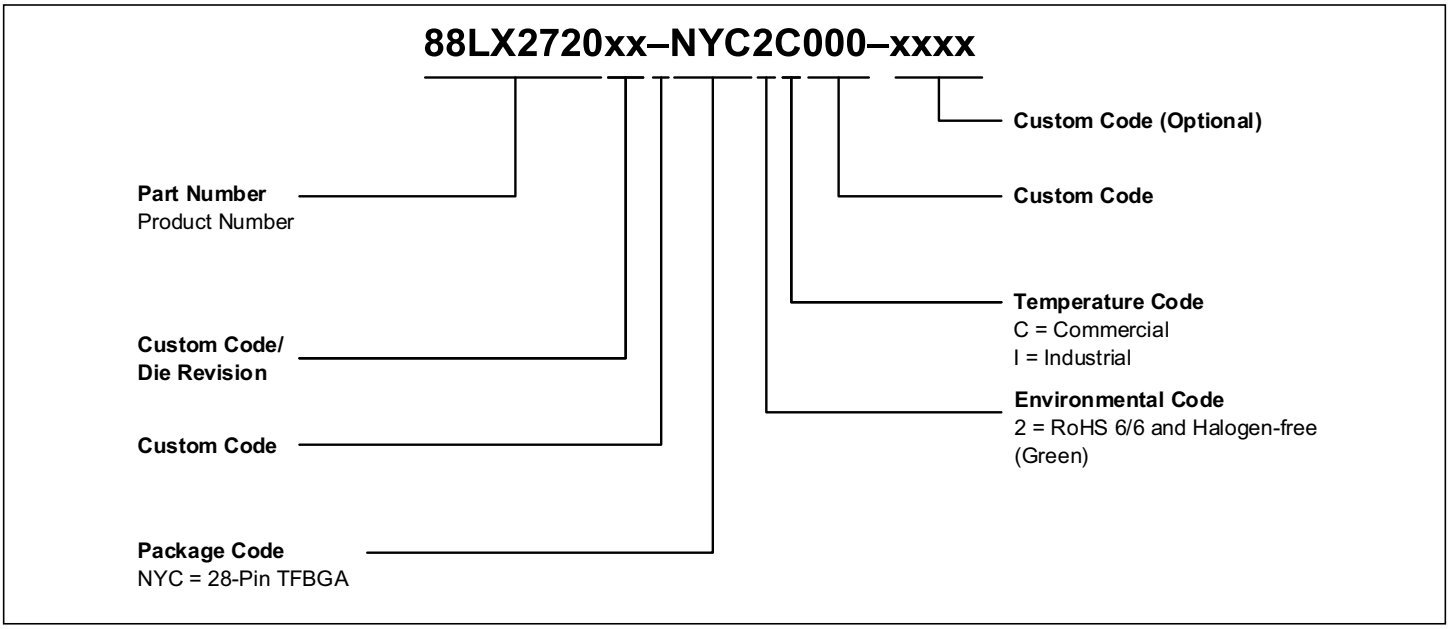

Figure 10: 88LX2720 Sample Part Number

Table 12: 88LX2720 Part Order Options

Package Type	Part Order Number	Description
28-Pin QFN	88LX2720A0-NYC2C000	G.hn Wave-2 AFE—single channel—powerline.

Package Marking

The following figure shows a sample commercial package marking and pin 1 location for the 88LX2720.

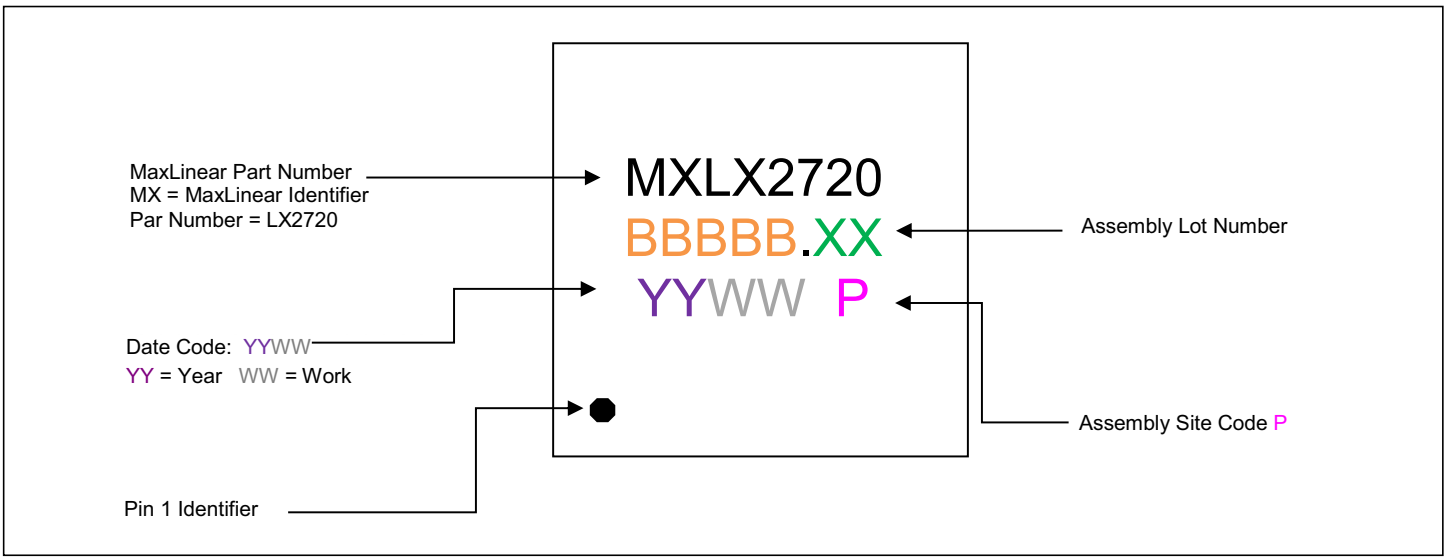

Figure 11: 88LX2720 Commercial Package Marking and Pin 1 Location

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