A New Direction in Mixed-Signal

# CLC2023

## Dual, Low Distortion, Low Offset, RRIO Amplifier

## General Description

The CLC2023 is a dual channel, high-performance, voltage feedback amplifier with low input voltage noise and ultra low distortion. The CLC2023 offers 6mV maximum input offset voltage, 3.5nV/√Hz broadband input voltage noise, and 0.00005% THD at 1kHz. It also provides 55MHz gain bandwidth product and 12V/µs slew rate making them well suited for applications requiring precision DC performance and high AC performance. This high-performance amplifier also offers a rail-to-rail input and output, simplifying single supply designs and offering larger dynamic range possibilities. The input range extends beyond the rails by 300mV.

The CLC2023 is designed to operate from 2.5V to 12V supplies and operate over the extended temperature range of -40°C to +125°.

### FEATURES

- 6mV maximum input offset voltage
- 0.00005% THD at 1kHz
- 5.3nV/√Hz input voltage noise > 10kHz
- -90dB/-85dB HD2/HD3 at 100kHz, $R_L$ = 100Ω
- <-100dB HD2 and HD3 at 10kHz, $R_L$ = 1kΩ
- Rail-to-rail input and output
- 55MHz unity gain bandwidth
- 12V/µs slew rate
- -40°C to +125°C operating temperature range
- Fully specified at 3 and ±5V supplies
- CLC2023: ROHS compliant MSOP-8, SOIC-8 package options

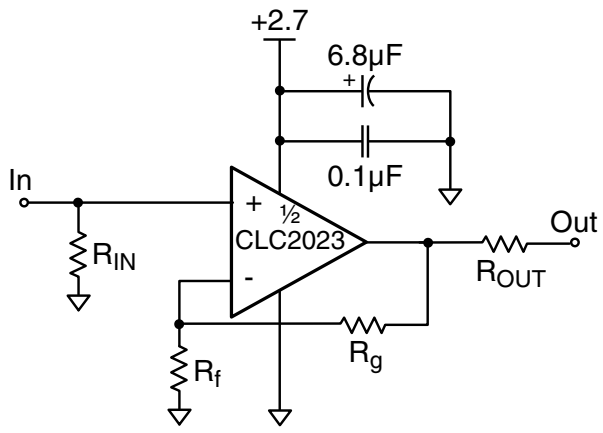
### APPLICATIONS

- Active filters
- Sensor interface
- HIgh-speed transducer amp
- Medical instrumentation
- Probe equipment
- Test equipment
- Smoke detectors
- Hand-held analytic instruments
- Current sense applications

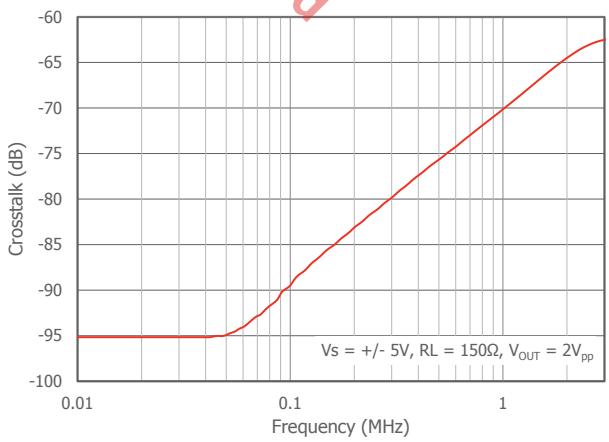
Ordering Information - back page

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## Typical Application




## Crosstalk vs. Frequency




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## Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

$V_S$ ..... 0V to +14V

$V_{IN}$ ..... $-V_S$ - 0.5V to $+V_S$ +0.5V

## Operating Conditions

Supply Voltage Range ..... 2.5V to 12V

Operating Temperature Range .....-40°C to 125°C

Junction Temperature .....150°C

Storage Temperature Range.....-65°C to 150°C

Lead Temperature (Soldering, 10s) .....260°C

## Package Thermal Resistance

$\theta_{JA}$ (MSOP-8) ..... 200°C/W

$\theta_{JA}$ (SOIC-8).....150°C/W

Package thermal resistance ($\theta_{JA}$), JEDEC standard, multi-layer test boards, still air.

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## Electrical Characteristics at +3V

$T_A$ = 25°C, $V_S$ = +3V, $R_f$ = 1kΩ, $R_L$ = 1kΩ to $V_S$/2; G = 2; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Frequency Domain Response | | | | | | |
| GBWP | -3dB Gain Bandwidth Product | G = 10, $V_{OUT}$ = 0.05$V_{pp}$ | | 31 | | MHz |
| UGBW | Unity Gain Bandwidth | $V_{OUT}$ = 0.05$V_{pp}$, $R_f$ = 0 | | 50 | | MHz |
| $BW_{SS}$ | -3dB Bandwidth | $V_{OUT}$ = 0.05$V_{pp}$ | | 24 | | MHz |
| $BW_{LS}$ | Large Signal Bandwidth | $V_{OUT}$ = 2$V_{pp}$ | | 3.3 | | MHz |
| Time Domain | | | | | | |
| $t_R$, $t_F$ | Rise and Fall Time | $V_{OUT}$ = 2V step; (10% to 90%) | | 150 | | ns |
| $t_S$ | Settling Time to 0.1% | $V_{OUT}$ = 2V step | | 78 | | ns |
| OS | Overshoot | $V_{OUT}$ = 2V step | | 0.3 | | % |
| SR | Slew Rate | 2V step | | 11 | | V/µs |
| Distortion/Noise Response | | | | | | |
| HD2 | 2nd Harmonic Distortion | 2$V_{pp}$, 10kHz, $R_L$ = 1kΩ | | -98 | | dBc |
| | | 2$V_{pp}$, 100kHz, $R_L$ = 100Ω | | -85 | | dBc |
| HD3 | 3rd Harmonic Distortion | 2$V_{pp}$, 10kHz, $R_L$ = 1kΩ | | -95 | | dBc |
| | | 2$V_{pp}$, 100kHz, $R_L$ = 100Ω | | -81 | | dBc |
| THD | Total Harmonic Distortion | 1$V_{pp}$, 1kHz, G = 1, $R_L$ = 2kΩ | | 0.0005 | | % |
| $e_n$ | Input Voltage Noise | >10kHz | | 5.5 | | nV/√Hz |
| | | >100kHz | | 3.9 | | nV/√Hz |
| $X_{TALK}$ | Crosstalk | 1MHz | | 70 | | dB |
| DC Performance | | | | | | |
| $V_{IO}$ | Input Offset Voltage | | | 0.088 | | mV |
| $d_{VIO}$ | Average Drift | | | 1.3 | | µV/°C |
| $I_B$ | Input Bias Current | | | -0.340 | | µA |
| $dI_B$ | Average Drift | | | 0.8 | | nA/°C |
| $I_{OS}$ | Input Offset Current | | | 0.2 | | µA |
| PSRR | Power Supply Rejection Ratio | DC | | 100 | | dB |
| $A_{OL}$ | Open Loop Gain | $V_{OUT}$ = $V_S$ / 2 | | 104 | | dB |
| $I_S$ | Supply Current | per channel | | 1.85 | | mA |
| Input Characteristics | | | | | | |
| $R_{IN}$ | Input Resistance | Non-inverting, G = 1 | | 30 | | MΩ |
| $C_{IN}$ | Input Capacitance | | | 1.1 | | pF |
| CMIR | Common Mode Input Range | | | -0.3 to 3.3 | | V |
| CMRR | Common Mode Rejection Ratio | DC, $V_{CM}$ = 0.5V to 2.5V | | 75 | | dB |
| Output Characteristics | | | | | | |
| $V_{OUT}$ | Output Swing | $R_L$ = 150Ω | | 0.085 to 2.80 | | V |
| | | $R_L$ = 1kΩ | | 0.04 to 2.91 | | V |
| $I_{OUT}$ | Output Current | | | +57, -47 | | mA |
| $I_{SC}$ | Short Circuit Current | $V_{OUT}$ = $V_S$ / 2 | | +65, -52 | | mA |

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## Electrical Characteristics at ±5V

$T_A$ = 25°C, $V_S$ = ±5V, $R_f$ = 1kΩ, $R_L$ = 1kΩ to GND; G = 2; unless otherwise noted.

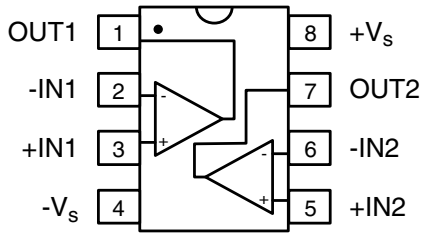
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Frequency Domain Response | | | | | | |
| GBWP | -3dB Gain Bandwidth Product | G = 10, $V_{OUT}$ = 0.05$V_{pp}$ | | 35 | | MHz |
| UGBW | Unity Gain Bandwidth | $V_{OUT}$ = 0.05$V_{pp}$, $R_f$ = 0 | | 55 | | MHz |
| $BW_{SS}$ | -3dB Bandwidth | $V_{OUT}$ = 0.05$V_{pp}$ | | 25 | | MHz |
| $BW_{LS}$ | Large Signal Bandwidth | $V_{OUT}$ = 2$V_{pp}$ | | 3.6 | | MHz |
| Time Domain | | | | | | |
| $t_R$, $t_F$ | Rise and Fall Time | $V_{OUT}$ = 2V step; (10% to 90%) | | 125 | | ns |
| $t_S$ | Settling Time to 0.1% | $V_{OUT}$ = 2V step | | 80 | | ns |
| OS | Overshoot | $V_{OUT}$ = 2V step | | 0.3 | | % |
| SR | Slew Rate | 4V step | | 12 | | V/µs |
| Distortion/Noise Response | | | | | | |
| HD2 | 2nd Harmonic Distortion | 2$V_{pp}$, 10kHz, $R_L$ = 1kΩ | | -125 | | dBc |
| | | 2$V_{pp}$, 100kHz, $R_L$ = 100Ω | | -90 | | dBc |
| HD3 | 3rd Harmonic Distortion | 2$V_{pp}$, 10kHz, $R_L$ = 1kΩ | | -127 | | dBc |
| | | 2$V_{pp}$, 100kHz, $R_L$ = 100Ω | | -85 | | dBc |
| THD | Total Harmonic Distortion | 1$V_{pp}$, 1kHz, G = 1, $R_L$ = 2kΩ | | 0.00005 | | % |
| $e_n$ | Input Voltage Noise | >10kHz | | 5.3 | | nV/√Hz |
| | | >100kHz | | 3.5 | | nV/√Hz |
| $X_{TALK}$ | Crosstalk | 1MHz | | 70 | | dB |
| DC Performance | | | | | | |
| $V_{IO}$ | Input Offset Voltage | | -6 | 0.050 | 6 | mV |
| $d_{VIO}$ | Average Drift | | | 1.3 | | µV/°C |
| $I_B$ | Input Bias Current | | -2.6 | -0.30 | 2.6 | µA |
| $dI_B$ | Average Drift | | | 0.85 | | nA/°C |
| $I_{OS}$ | Input Offset Current | | | 0.2 | 0.7 | µA |
| PSRR | Power Supply Rejection Ratio | DC | 82 | 100 | | dB |
| $A_{OL}$ | Open Loop Gain | $V_{OUT}$ = $V_S$ / 2 | 95 | 115 | | dB |
| $I_S$ | Supply Current | per channel | | 2.2 | 2.75 | mA |
| Input Characteristics | | | | | | |
| $R_{IN}$ | Input Resistance | Non-inverting, G = 1 | | 30 | | MΩ |
| $C_{IN}$ | Input Capacitance | | | 1 | | pF |
| CMIR | Common Mode Input Range | | | ±5.3 | | V |
| CMRR | Common Mode Rejection Ratio | DC, $V_{CM}$ = -3V to 3V | 70 | 85 | | dB |
| Output Characteristics | | | | | | |
| $V_{OUT}$ | Output Swing | $R_L$ = 150Ω | | -4.826 to 4.534 | | V |
| | | $R_L$ = 1kΩ | -4.7 | -4.93 to 4.85 | 4.7 | V |
| $I_{OUT}$ | Output Current | | | +60, -48 | | mA |
| $I_{SC}$ | Short Circuit Current | $V_{OUT}$ = $V_S$ / 2 | | +65, -52 | | mA |

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## CLC2023 Pin Configuration

### MSOP-8 / SOIC-8




## CLC2023 Pin Assignments

### MSOP-8 / SOIC-8

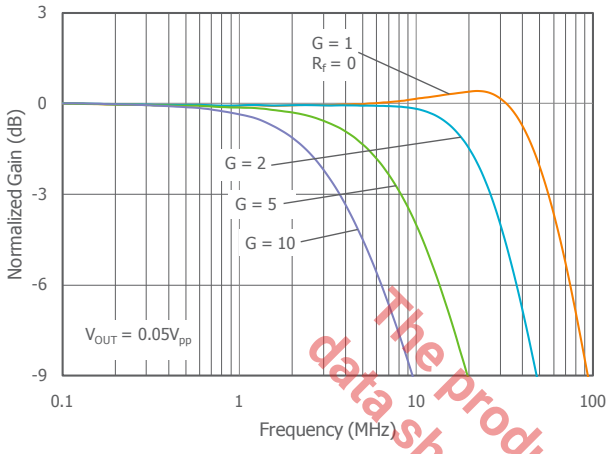
| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT1 | Output, channel 1 |
| 2 | -IN1 | Negative input, channel 1 |
| 3 | +IN1 | Positive input, channel 1 |
| 4 | $-V_S$ | Negative supply |
| 5 | +IN2 | Positive input, channel 2 |
| 6 | -IN2 | Negative input, channel 2 |
| 7 | OUT2 | Output, channel 2 |
| 8 | $+V_S$ | Positive supply |

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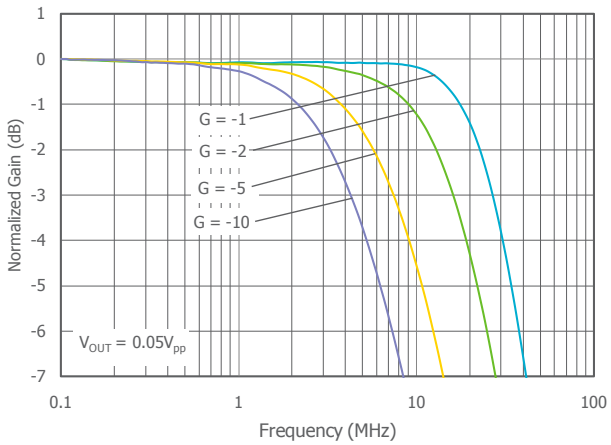
## Typical Performance Characteristics

$T_A$ = 25°C, $V_S$ = ±5V, $R_f$ = 1kΩ, $R_L$ = 1kΩ, G = 2; unless otherwise noted.

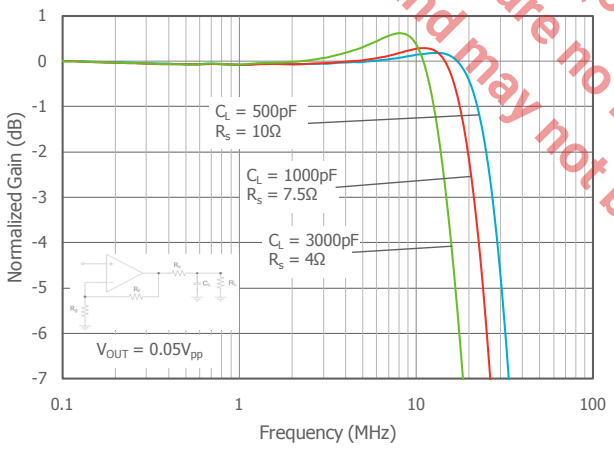
Non-Inverting Frequency Response



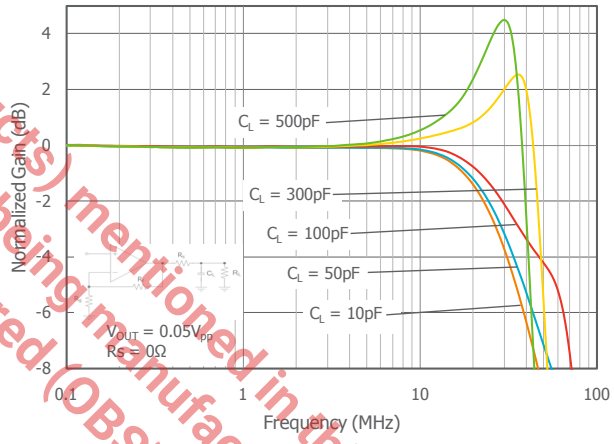

Inverting Frequency Response



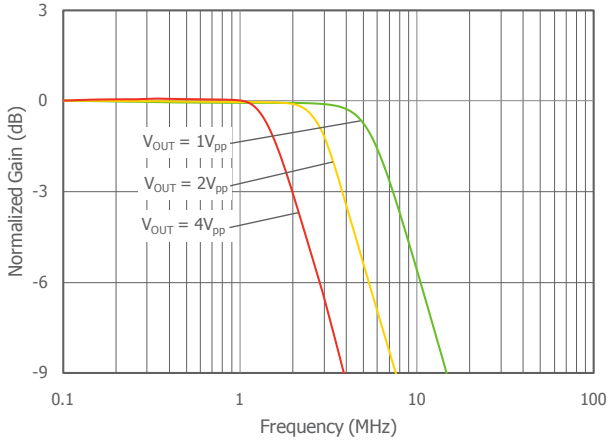

Frequency Response vs. $C_L$



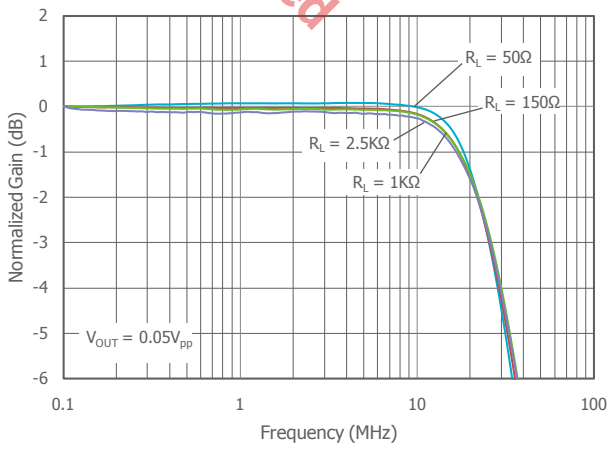

Frequency Response vs. $C_L$ without $R_S$




Frequency Response vs. $V_{OUT}$




Frequency Response vs. $R_L$

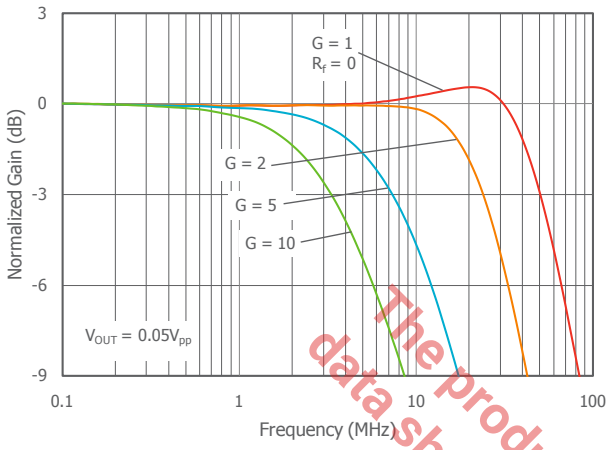



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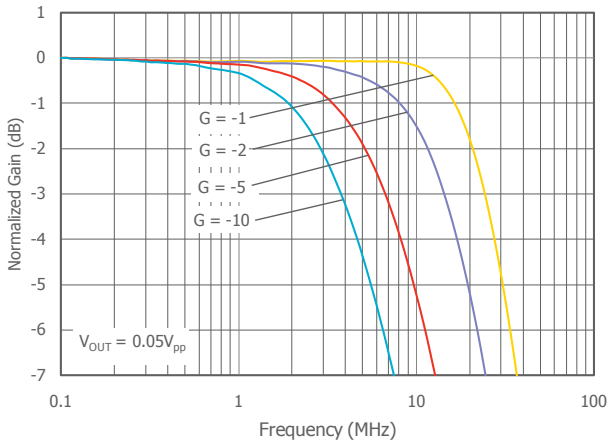
## Typical Performance Characteristics

$T_A$ = 25°C, $V_S$ = ±5V, $R_f$ = 1kΩ, $R_L$ = 1kΩ, G = 2; unless otherwise noted.

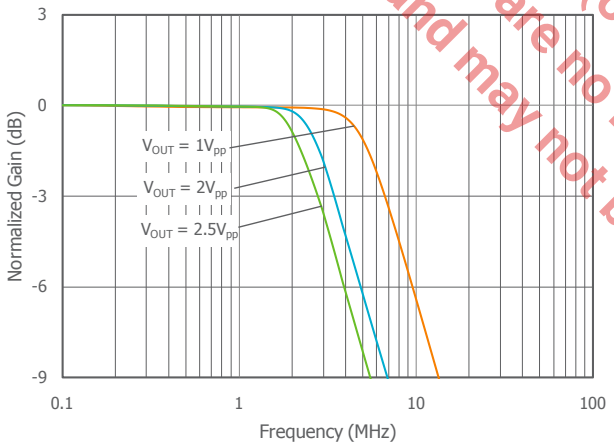
Non-Inverting Frequency Response at $V_S$ = 3V



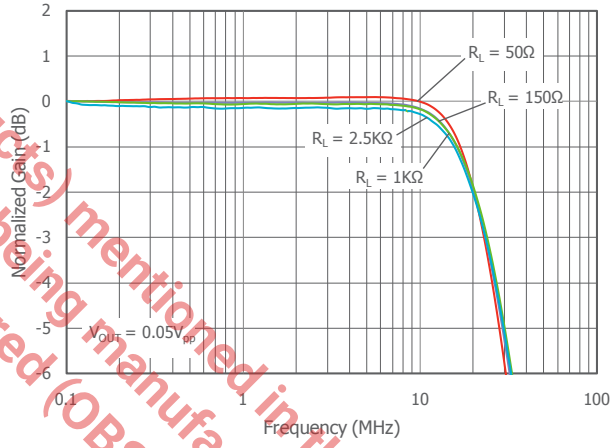

Inverting Frequency Response at $V_S$ = 3V



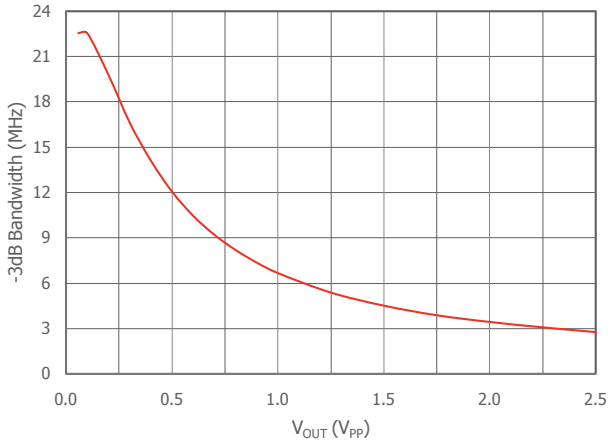

Frequency Response vs. $V_{OUT}$ at $V_S$ = 3V



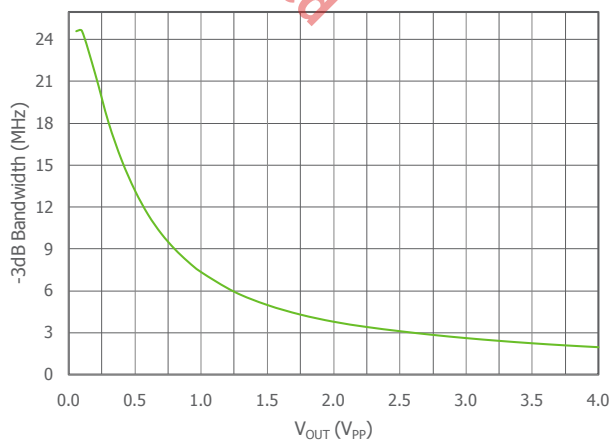

Frequency Response vs. $R_L$ at $V_S$ = 3V




-3dB Bandwidth vs. Output Voltage at $V_S$ = 3V




-3dB Bandwidth vs. Output Voltage

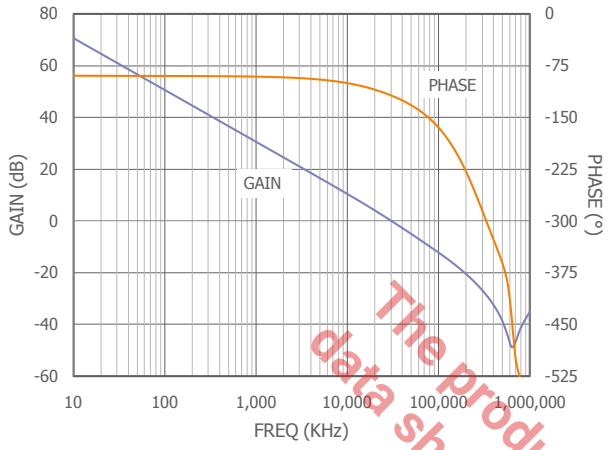



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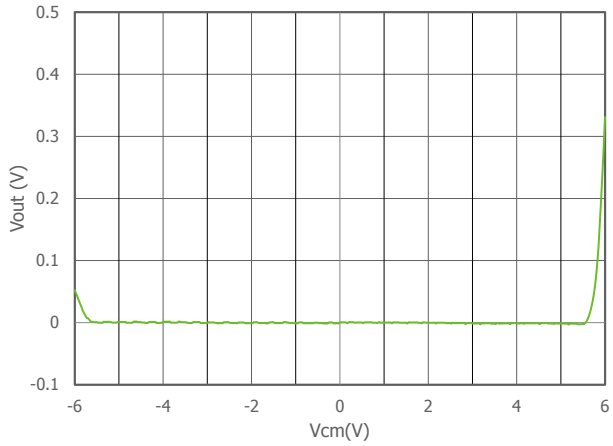
## Typical Performance Characteristics

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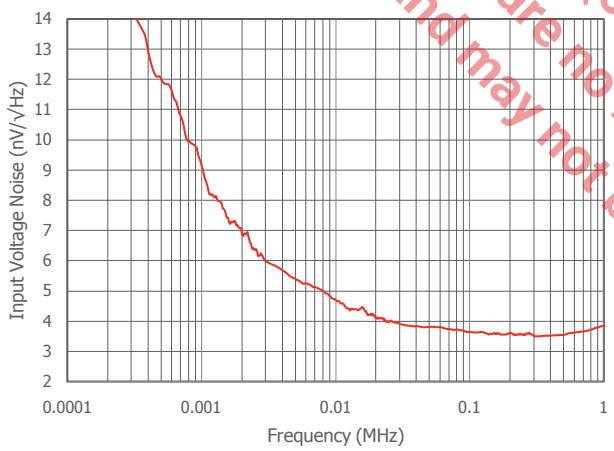
Open Loop Gain and Phase vs.



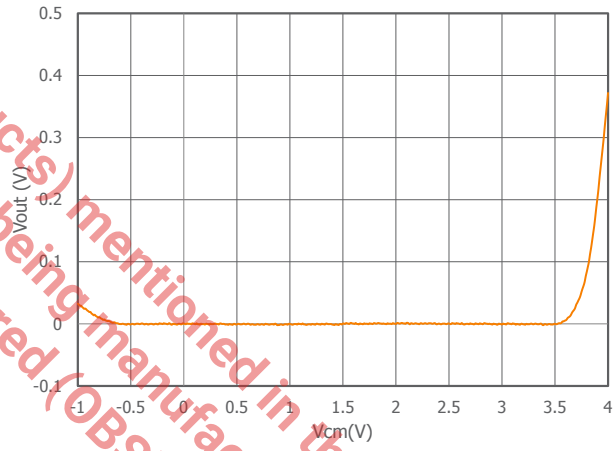

CMIR



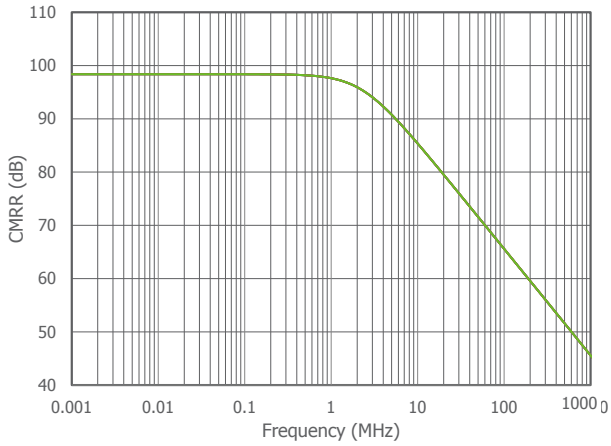

Input Voltage Noise



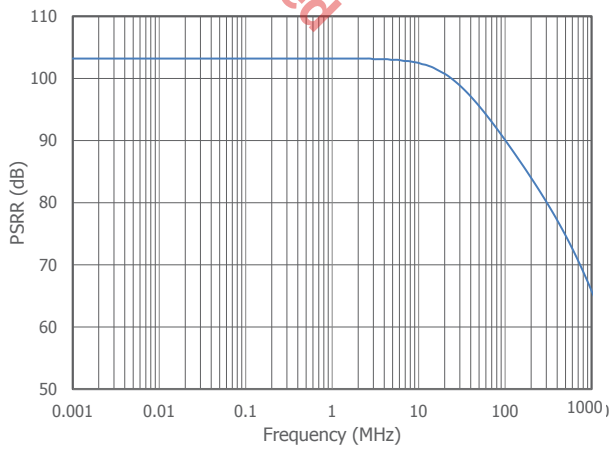

CMIR at $V_S$ = 3V




CMRR vs. Frequency




PSRR vs. Frequency



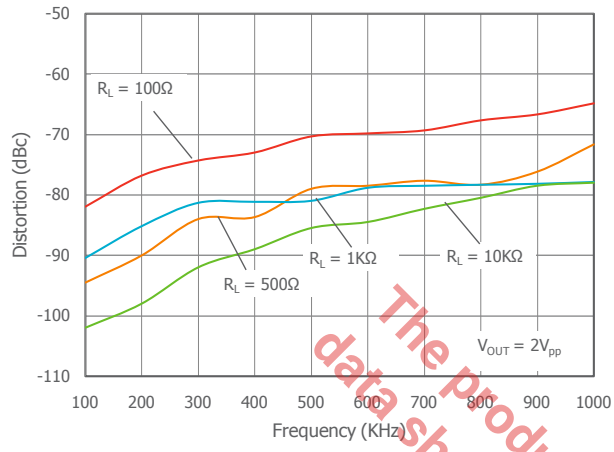

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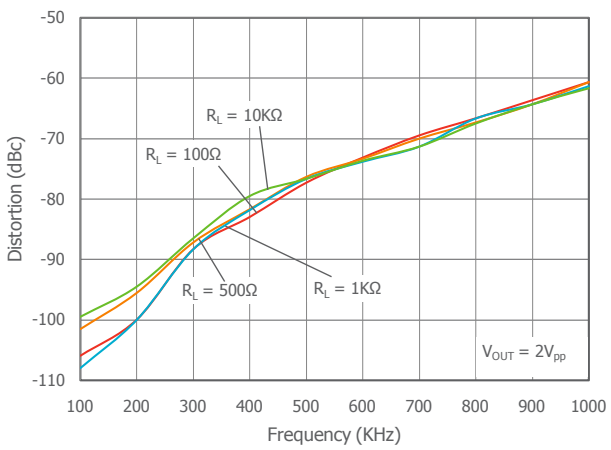
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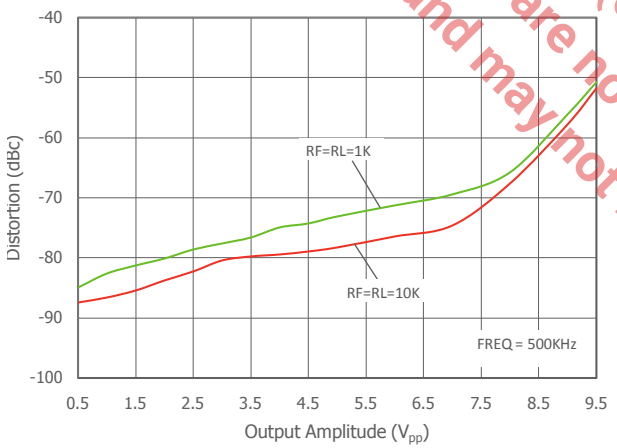
2nd Harmonic Distortion vs. $R_L$



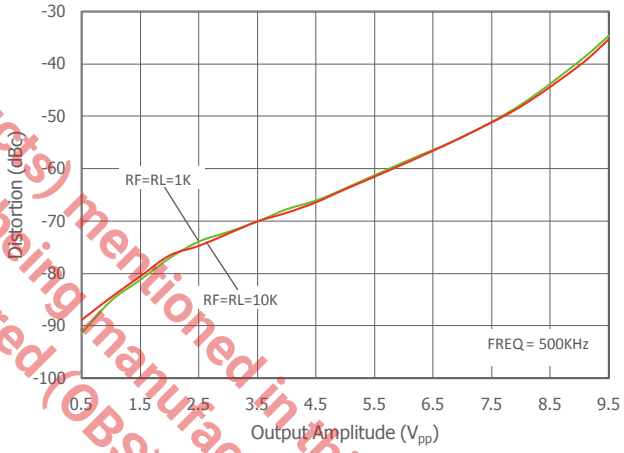

3rd Harmonic Distortion vs. $R_L$



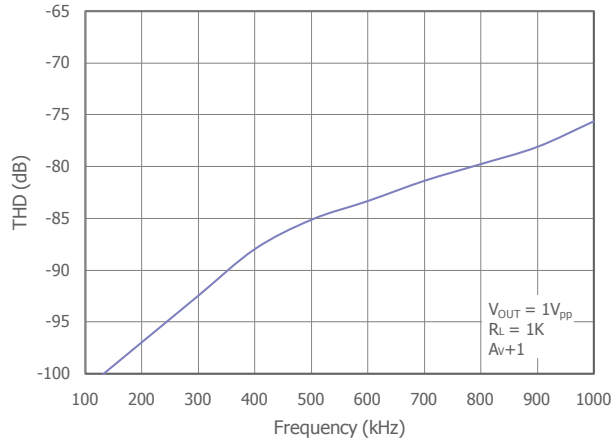

2nd Harmonic Distortion vs. $V_{OUT}$




3rd Harmonic Distortion vs. $V_{OUT}$




THD vs. Frequency

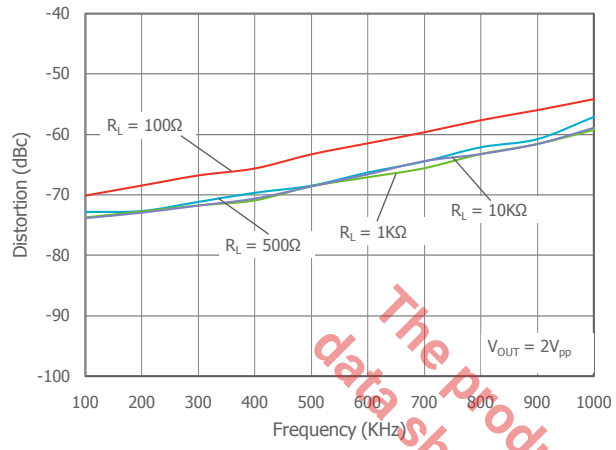



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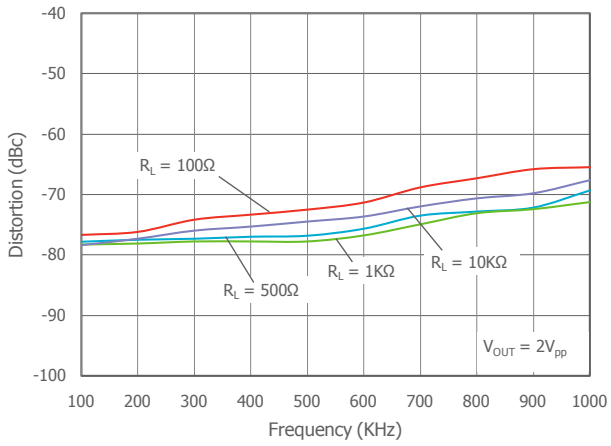
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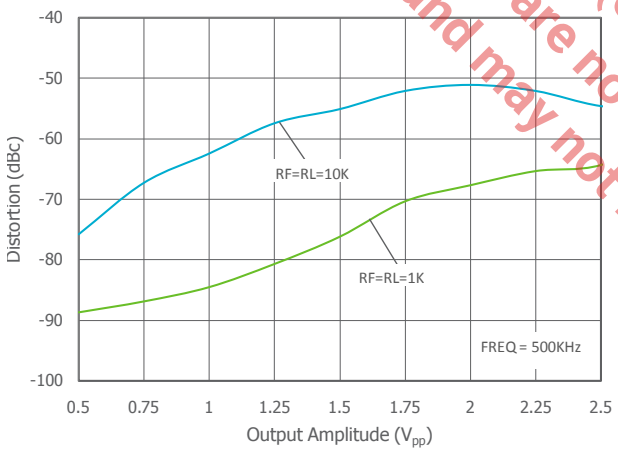
2nd Harmonic Distortion vs. $R_L$ at $V_S$ = 3V



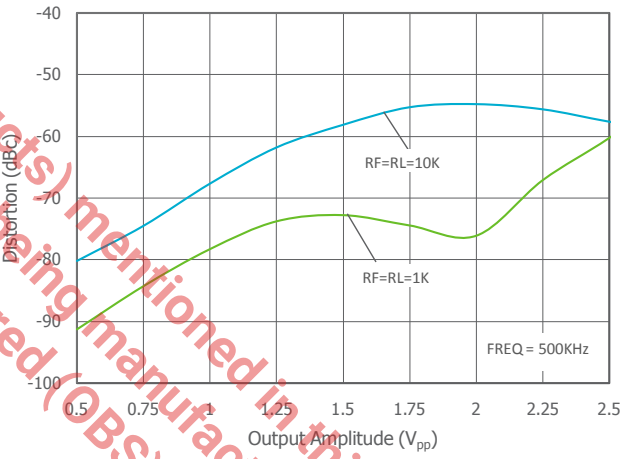

3rd Harmonic Distortion vs. $R_L$ at $V_S$ = 3V



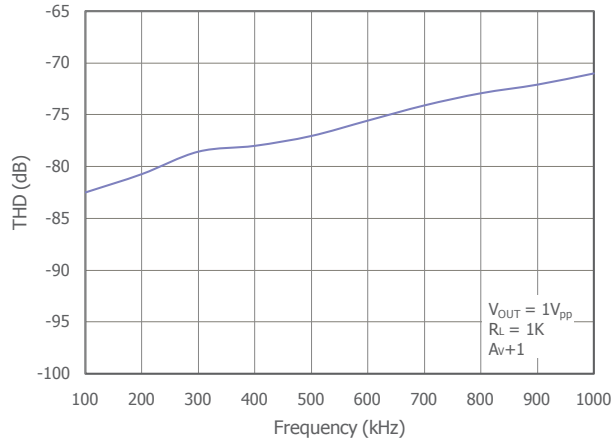

2nd Harmonic Distortion vs. $V_{OUT}$ at $V_S$ = 3V




3rd Harmonic Distortion vs. $V_{OUT}$ at $V_S$ = 3V




THD vs. Frequency at $V_S$ = 3V

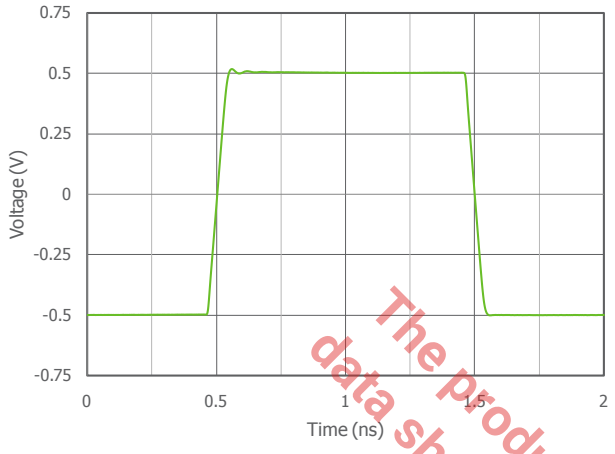



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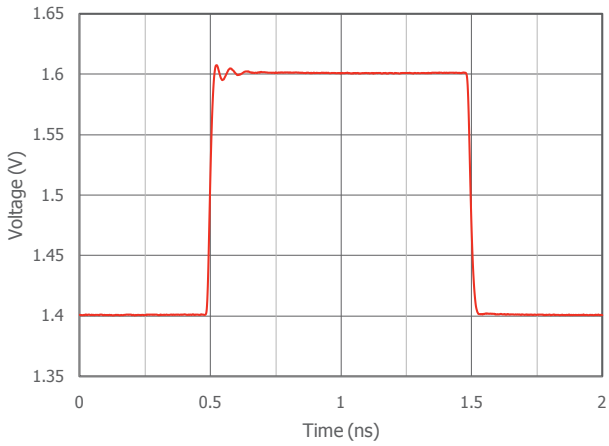
## Typical Performance Characteristics

$T_A$ = 25°C, $V_S$ = ±5V, $R_f$ = 1kΩ, $R_L$ = 1kΩ, G = 2; unless otherwise noted.

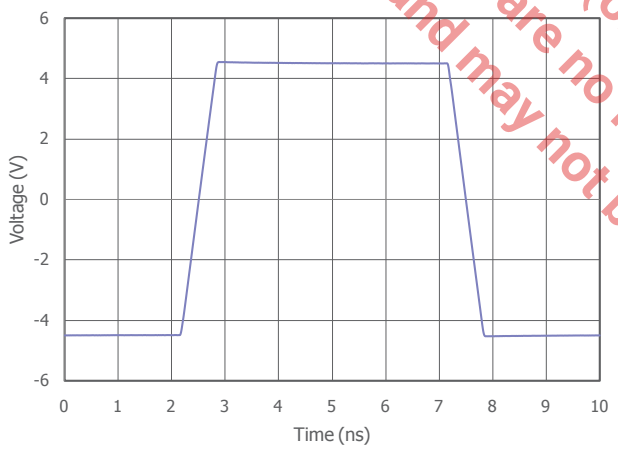
Small Signal Pulse Response



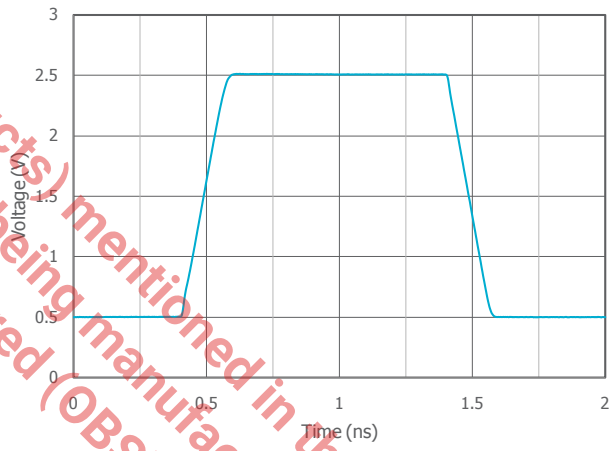

Small Signal Pulse Response at $V_S$ = 3V




Large Signal Pulse Response




Large Signal Pulse Response at $V_S$ = 3V




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## Application Information

### Basic Information

Figures 1 and 2 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

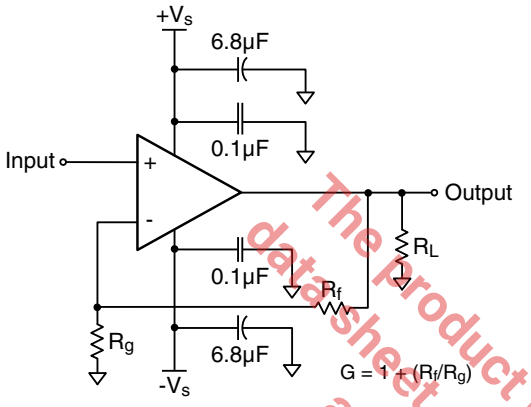



Figure 1: Typical Non-Inverting Gain Circuit

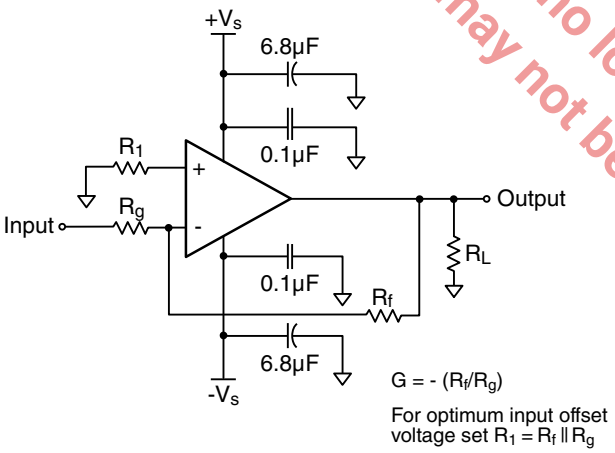



Figure 2: Typical Inverting Gain Circuit

### Power Dissipation

Power dissipation should not be a factor when operating under the stated 500Ω load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ ($\theta_{JA}$) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine $P_D$, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMSsupply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{load})_{RMS^2})/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in Figure 2 would be calculated as:

$$R_L \,||\, (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, $P_D$ can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{load}$$

Quiescent power can be derived from the specified $I_S$ values along with known supply voltage, $V_{supply}$. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{load})_{RMS} = V_{peak} / \sqrt{2}$$

$$(I_{load})_{RMS} = (V_{load})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{Dynamic} = (V_{S+} - V_{load})_{RMS} \times (I_{load})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

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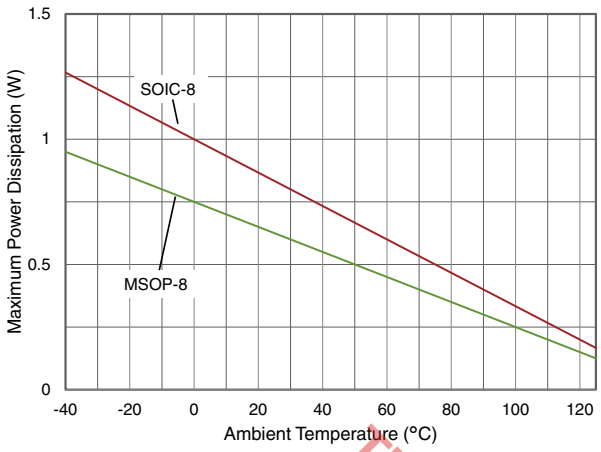



Figure 3. Maximum Power Derating

## Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, $R_S$, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 4.

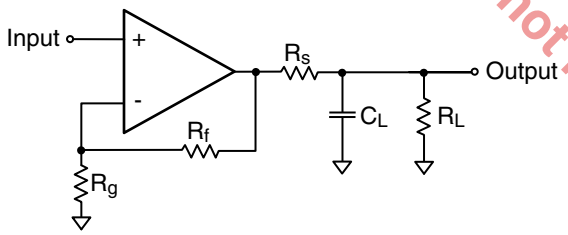



Figure 4. Addition of $R_S$ for Driving Capacitive Loads

The CLC2023 is capable of driving up to 300pF directly, with no series resistance. Directly driving 500pF causes over 4dB of frequency peaking, as shown in the plot on page 6. Table 1 provides the recommended $R_S$ for various capacitive loads. The recommended $R_S$ values result in ≤ 1dB peaking in the frequency response. The Frequency Response vs. $C_L$ plots, on page 6, illustrate the response of the CLC2023.

| $C_L$ (pF) | $R_S$ (Ω) | -3dB BW (MHz) |
|---|---|---|
| 500 | 10 | 27 |
| 1000 | 7.5 | 20 |
| 3000 | 4 | 15 |

Table 1: Recommended $R_S$ vs. $C_L$

For a given load capacitance, adjust $R_S$ to optimize the tradeoff between settling time and bandwidth. In general, reducing $R_S$ will increase bandwidth at the expense of additional overshoot and ringing.

## Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The CLC2023 will typically recover in less than 20ns from an overdrive condition. Figure 5 shows the CLC2023 in an overdriven condition.

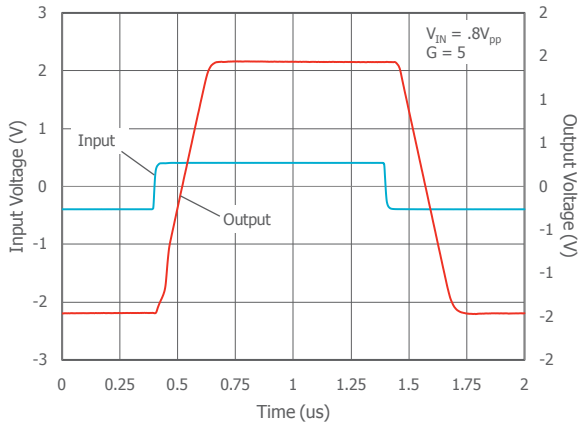



Figure 5: Overdrive Recovery

## Considerations for Offset and Noise Performance

### Offset Analysis

There are three sources of offset contribution to consider; input bias current, input bias current mismatch, and input offset voltage. The input bias currents are assumed to be equal with and additional offset current in one of the inputs to account for mismatch. The bias currents will not affect the offset as long as the parallel combination of $R_f$ and $R_g$ matches $R_t$. Refer to Figure 6.

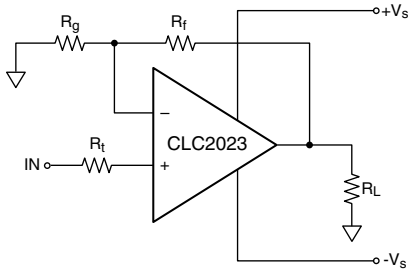



Figure 6: Circuit for Evaluating Offset

The first place to start is to determine the source resistance. If it is very small an additional resistance may need to be added to keep the values of $R_f$ and $R_g$ to practical levels. For this analysis we assume that $R_t$ is the total resistance present on the non-inverting input. This gives us one equation that we must solve:

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$$R_t = R_g || R_f$$

This equation can be rearranged to solve for $R_g$:

$$R_g = (R_t * R_f) / (R_f - R_t)$$

The other consideration is desired gain (G) which is:

$$G = (1 + R_f/R_g)$$

By plugging in the value for $R_g$ we get

$$R_f = G * R_t$$

And $R_g$ can be written in terms of $R_t$ and G as follows:

$$R_g = (G * R_t) / (G - 1)$$

The complete input offset equation is now only dependent on the voltage offset and input offset terms given by:

$$VI_{OS} = \sqrt{\left(V_{IO}\right)^2 + \left(I_{OS} * RT\right)^2}$$

And the output offset is:

$$VO_{OS} = G * \sqrt{\left(V_{IO}\right)^2 + \left(I_{OS} * RT\right)^2}$$

## Noise analysis

The complete equivalent noise circuit is shown in Figure 7.

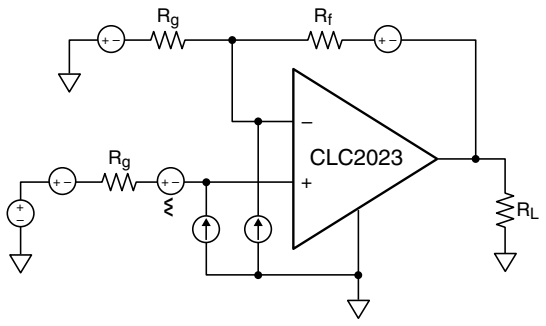



Figure 7: Complete Equivalent Noise Circuit

The complete noise equation is given by:

$$v_o^2 = v_{orext}^2 + \left(e_n\left(1 + \frac{RF}{RG}\right)\right)^2 + \left(i_{bp} * RT\left(1 + \frac{RF}{RG}\right)\right)^2 + \left(i_{bn} * RF\right)^2$$

Where $V_{orext}$ is the noise due to the external resistors and is given by:

$$v_o^2 = \left(e_n\left(1 + \frac{RF}{RG}\right)\right)^2 + \left(e_G * \frac{RF}{RG}\right)^2 + e_F^2$$

The complete equation can be simplified to:

$$v_o^2 = 3 * \left(4kT * G * RT\right) + \left(e_n G\right)^2 + 2 * \left(i_n * RT\right)^2$$

It's easy to see that the effect of amplifier voltage noise is proportionate to gain and will tend to dominate at large gains. The other terms will have their greatest impact at large $R_t$ values at lower gains.

## Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

## Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

| Evaluation Board # | Products |
|---|---|
| CEB006 | CLC2023 in SOIC-8 |
| CEB010 | CLC2023 in MSOP-8 |

## Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 8-12 These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short $-V_S$ to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

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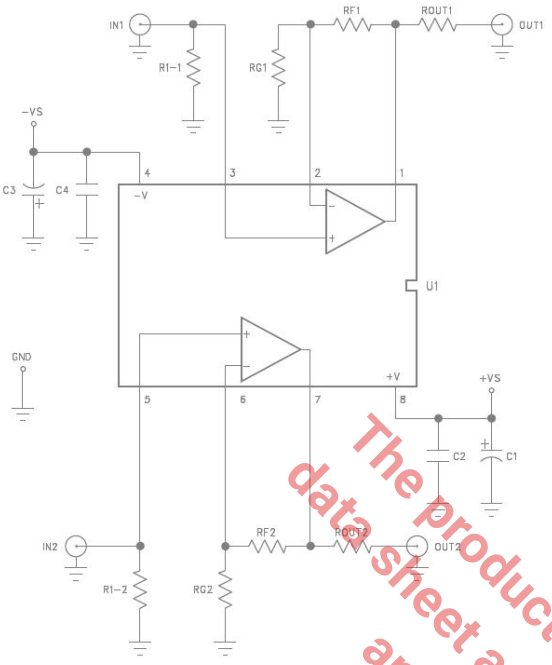



Figure 8. CEB006 & CEB010 Schematic

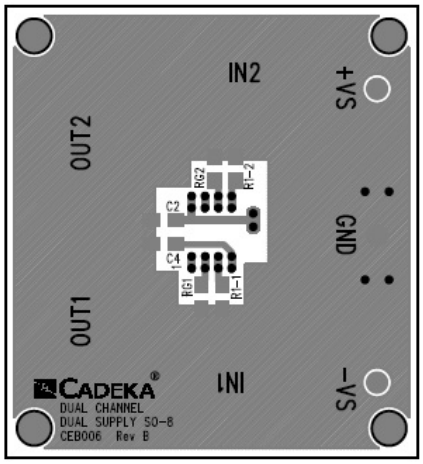



Figure 9. CEB006 Top View

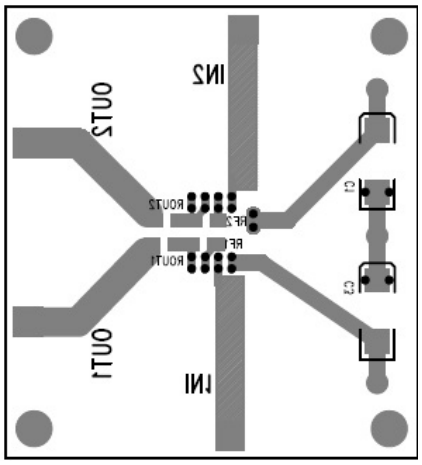



Figure 10. CEB006 Bottom View

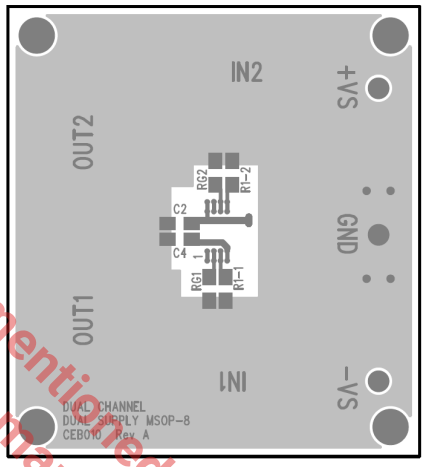



Figure 11. CEB010 Top View

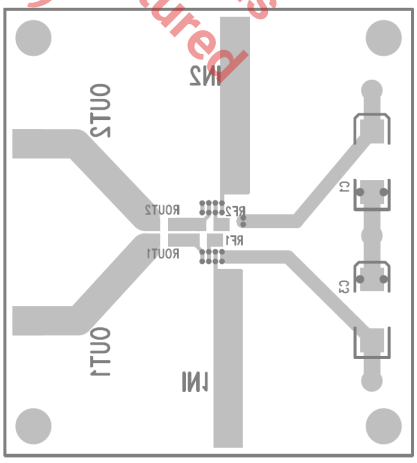
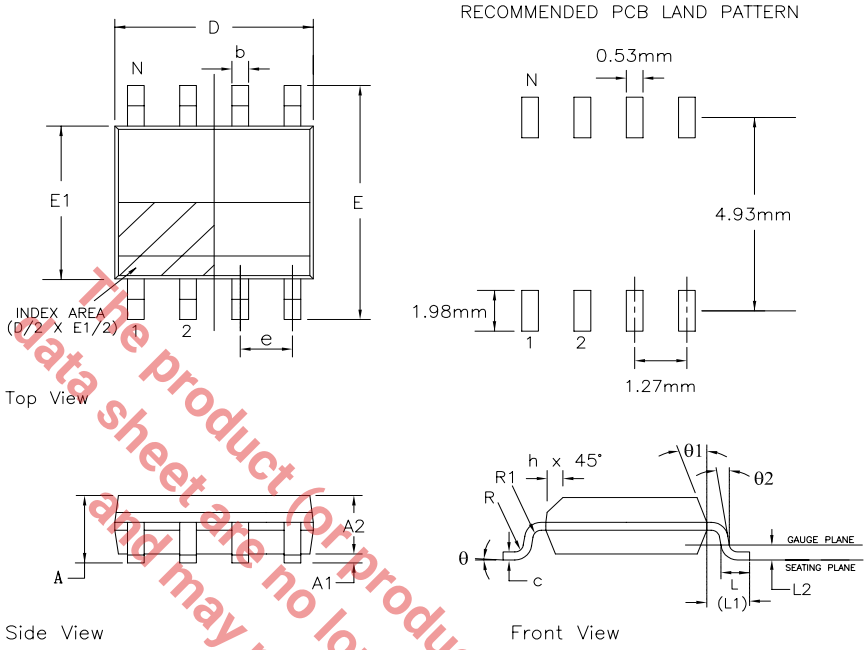



Figure 12. CEB010 Bottom View

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# Mechanical Dimensions

## SOIC-8 Package

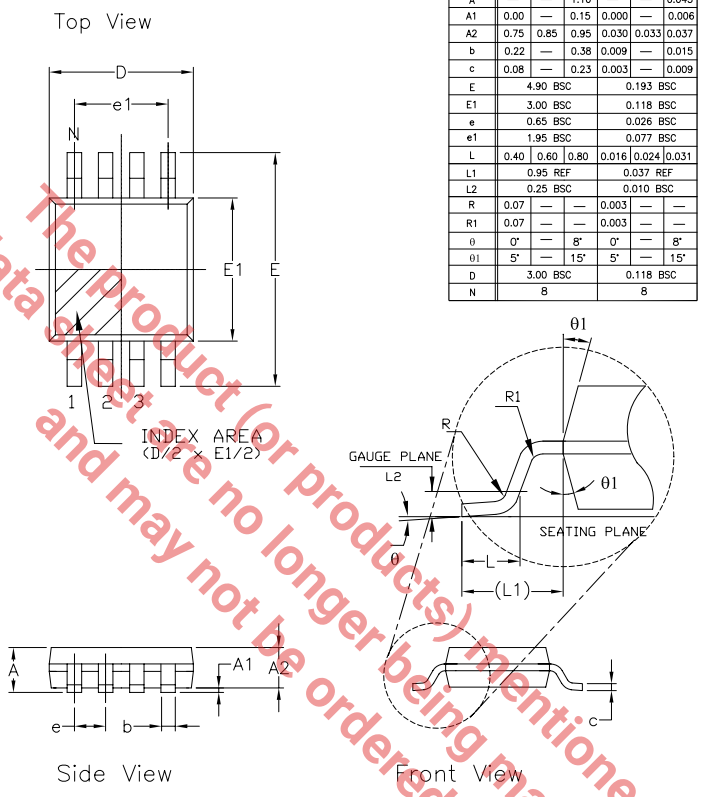



| 8 Pin SOICN JEDEC MS-012 Variation AA | | | | | | | |
|---|---|---|---|---|---|---|---|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | | |
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| A | 1.35 | — | 1.75 | 0.053 | — | 0.069 | |
| A1 | 0.10 | — | 0.25 | 0.004 | — | 0.010 | |
| A2 | 1.25 | — | 1.65 | 0.049 | — | 0.065 | |
| b | 0.31 | — | 0.51 | 0.012 | — | 0.020 | |
| c | 0.17 | — | 0.25 | 0.007 | — | 0.010 | |
| E | 6.00 BSC | | | 0.236 BSC | | | |
| E1 | 3.90 BSC | | | 0.154 BSC | | | |
| e | 1.27 BSC | | | 0.050 BSC | | | |
| h | 0.25 | — | 0.50 | 0.010 | — | 0.020 | |
| L | 0.40 | — | 1.27 | 0.016 | — | 0.050 | |
| L1 | 1.04 REF | | | 0.041 REF | | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | | |
| R | 0.07 | — | — | 0.003 | — | — | |
| R1 | 0.07 | — | — | 0.003 | — | — | |
| θ | 0° | — | 8° | 0° | — | 8° | |
| θ1 | 5° | — | 15° | 5° | — | 15° | |
| θ2 | 0° | — | — | 0° | — | — | |
| D | 4.90 BSC | | | 0.193 BSC | | | |
| N | 8 | | | 8 | | | |

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## MSOP-8 Package

| 8 Pin MSOP JEDEC MO-187 Variation AA | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | — | — | 1.10 | — | — | 0.043 |
| A1 | 0.00 | — | 0.15 | 0.000 | — | 0.006 |
| A2 | 0.75 | 0.85 | 0.95 | 0.030 | 0.033 | 0.037 |
| b | 0.22 | — | 0.38 | 0.009 | — | 0.015 |
| c | 0.08 | — | 0.23 | 0.003 | — | 0.009 |
| E | 4.90 BSC | | | 0.193 BSC | | |
| E1 | 3.00 BSC | | | 0.118 BSC | | |
| e | 0.65 BSC | | | 0.026 BSC | | |
| e1 | 1.95 BSC | | | 0.077 BSC | | |
| L | 0.40 | 0.60 | 0.80 | 0.016 | 0.024 | 0.031 |
| L1 | 0.95 REF | | | 0.037 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.07 | — | — | 0.003 | — | — |
| R1 | 0.07 | — | — | 0.003 | — | — |
| θ | 0° | — | 8° | 0° | — | 8° |
| θ1 | 5° | — | 15° | 5° | — | 15° |
| D | 3.00 BSC | | | 0.118 BSC | | |
| N | 8 | | | 8 | | |




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## Ordering Information

| Part Number | Package | Green | Operating Temperature Range | Packaging |
|---|---|---|---|---|
| CLC2023 Ordering Information | | | | |
| CLC2023IMP8X | MSOP-8 | Yes | -40°C to +125°C | Tape & Reel |
| CLC2023IMP8MTR | MSOP-8 | Yes | -40°C to +125°C | Mini Tape & Reel |
| CLC2023IMP8EVB | Evaluation Board | N/A | N/A | N/A |
| CLC2023ISO8X | SOIC-8 | Yes | -40°C to +125°C | Tape & Reel |
| CLC2023ISO8MTR | SOIC-8 | Yes | -40°C to +125°C | Mini Tape & Reel |
| CLC2023ISO8EVB | Evaluation Board | N/A | N/A | N/A |

Moisture sensitivity level for all parts is MSL-1.

## Revision History

| Revision | Date | Description |
|---|---|---|
| 1D (ECN 1451-06) | December 2014 | Reformat into Exar data sheet template. Updated ordering information table to include MTR and EVB part numbers. Increased "I" temperature range from +85 to +125°C. Removed "A" temp grade parts, since "I" is now equivalent. Updated thermal resistance numbers and package outline drawings. |

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A New Direction in Mixed-Signal

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